

Compal confidential

Hamburg 10ADG

NALAE LA-6054P Schematics Document

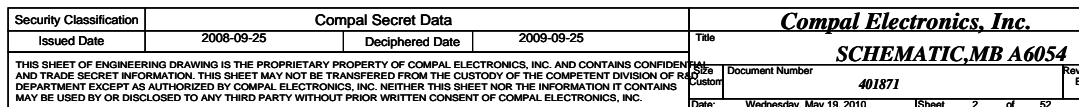
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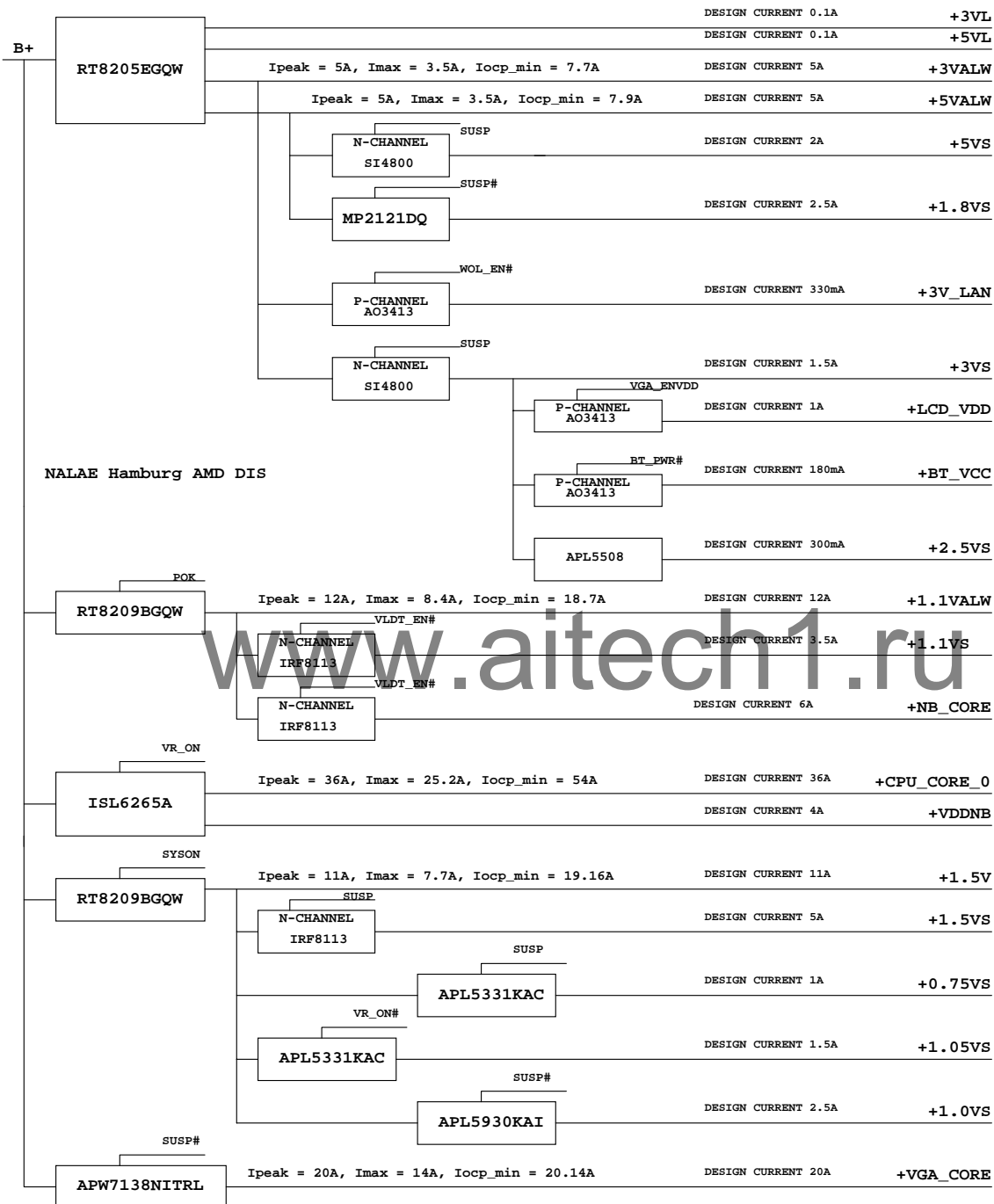
Mobile AMD S1G4/ RS880M / SB820M

2009-02-04 Rev. 0.2

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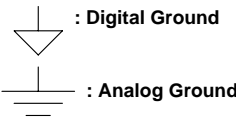
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Voltage Rails

O : ON
X : OFF

power plane	State	B+ +3VL +5VL +RTCVC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE +NB_CORE
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

Symbol Note :



@ : just reserve , no build

GPU	CPU	NB	VGA	SB	Comment
Manhattan	S1G4	RS880M	MADISON	SB820M	Madison @ or PARK @
	S1G4	RS880M	PARK	SB820M	+4PCS or 8PCS
M96/M92	S1G4	RS880M	M96	SB820M	M9X @+M96 @ or M92 @
	S1G4	RS880M	M92	SB820M	+4PCS or 8PCS

Platform	CPU	NB	VGA	SB	Comment
Danube					
	S1G4	RS880M	NA	SB820M	

BTO (Build-To-Order) Option Table

Function	BLUE TOOTH	HDMI				
Description	(B)	(Y)				
Explain						
BTO	BT@	H@				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC SM Bus1 address

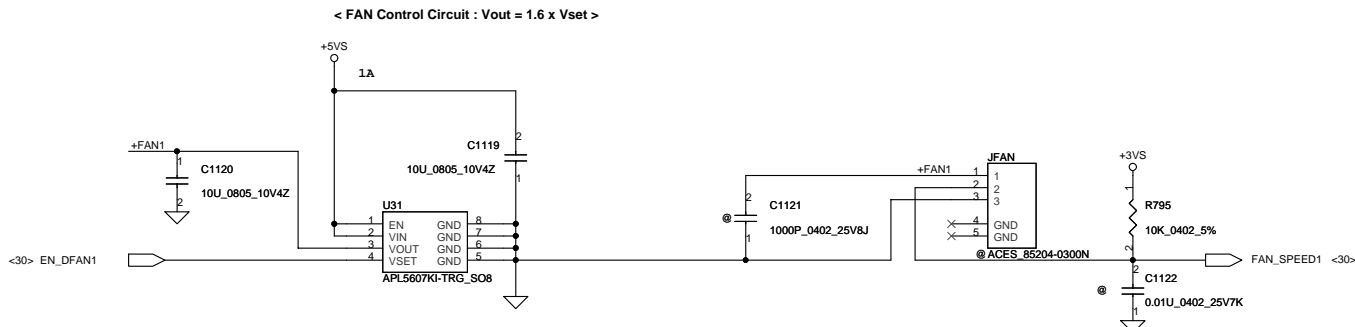
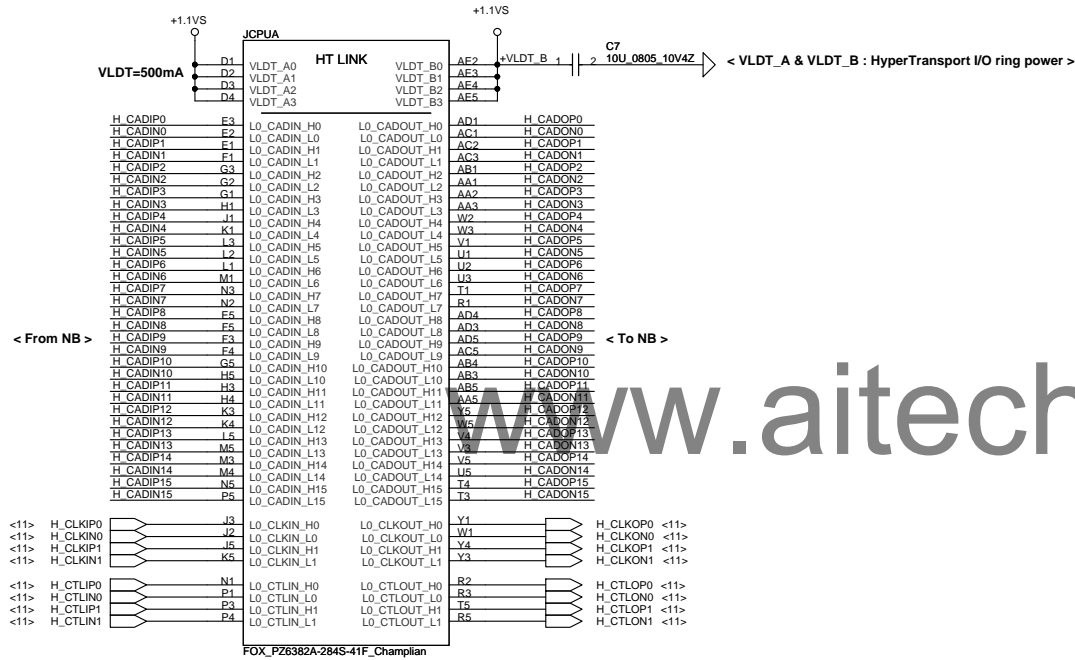
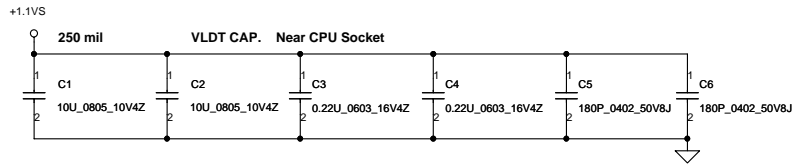
Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D4		

EC SM Bus2 address

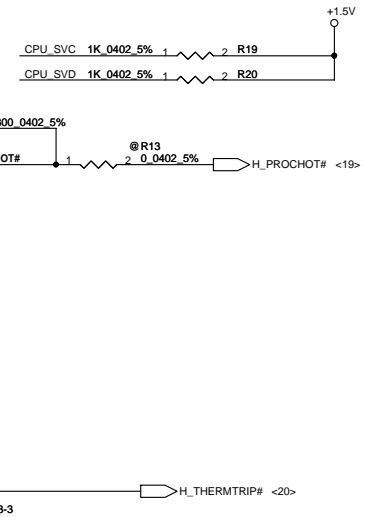
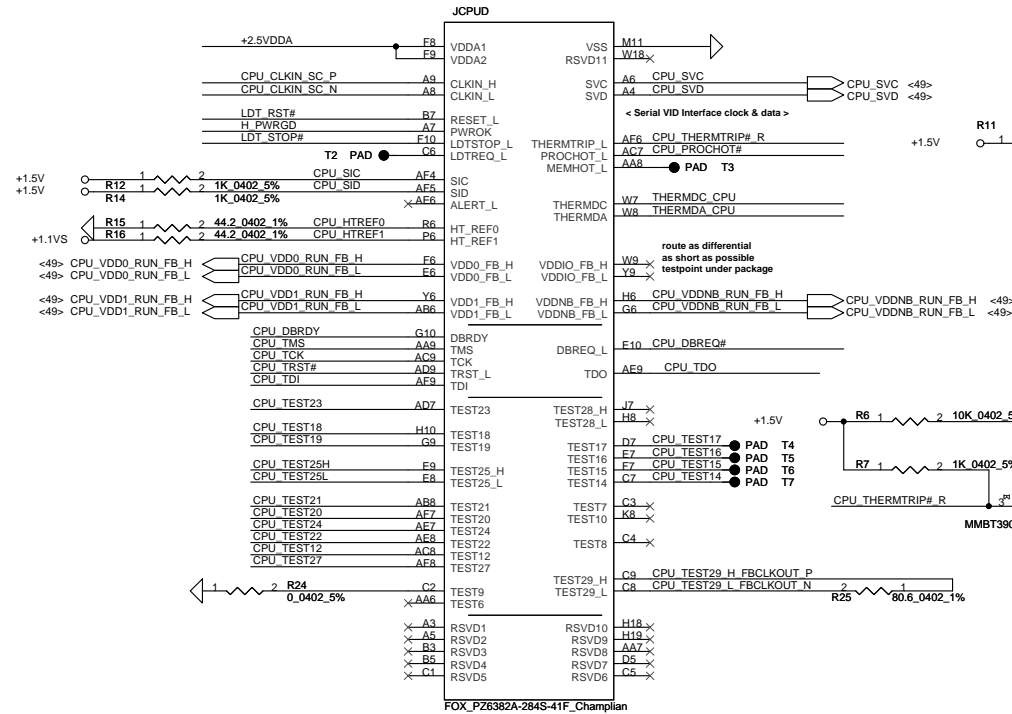
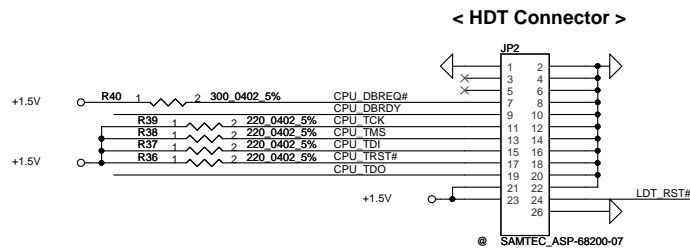
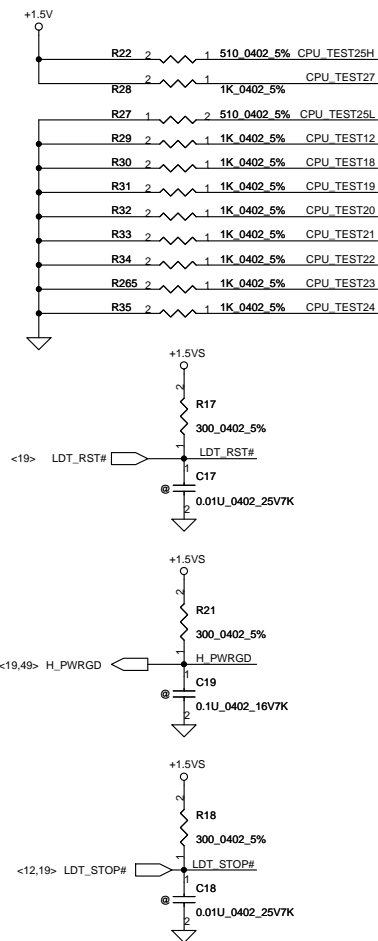
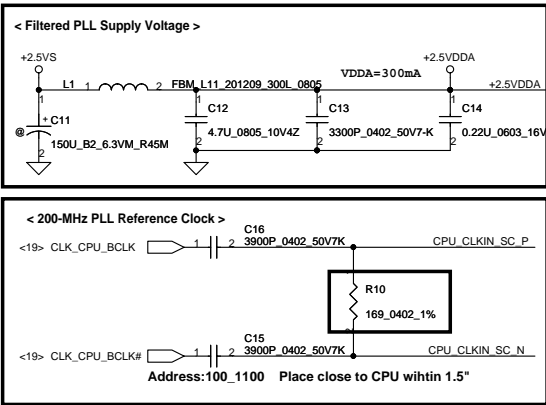
Device	HEX	Address
ADH1032-1 CPU	98H	1001 100X b
ADH1032-2 VGA	9AH	1001 101X b
EC KB926D3		

SMBUS Control Table

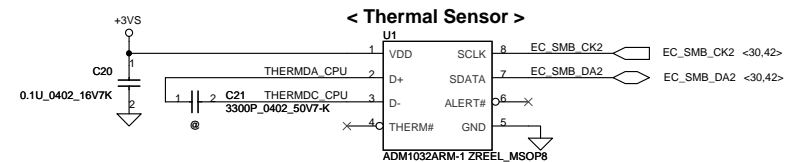
	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V						
EC_SMB_CK2 EC_SMB_DA2	KB926		V					
I2C_CLK I2C_DATA	RS880M						V	
DDC_CLK0 DDC_DATA0	RS880M							V
SCL0 SDA0	SB820			V	V			
SCL1 SDA1	SB820					V		



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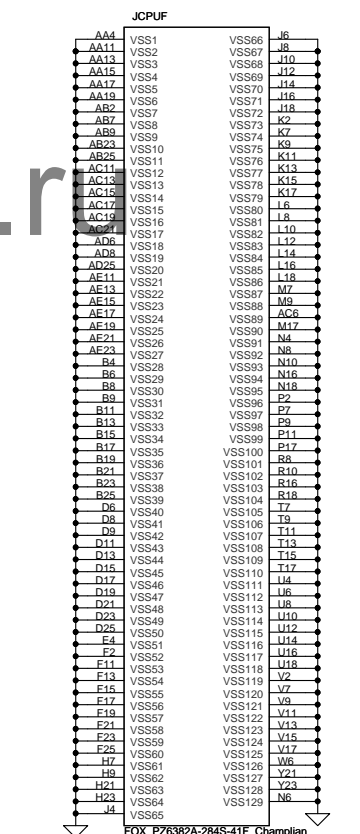
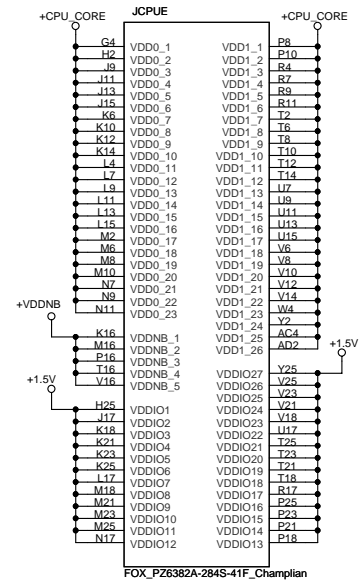
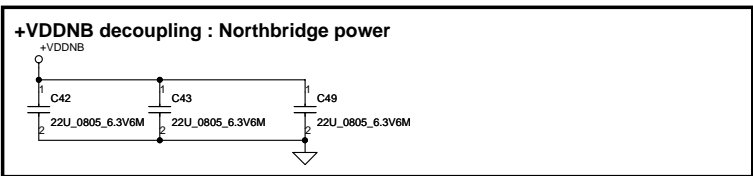
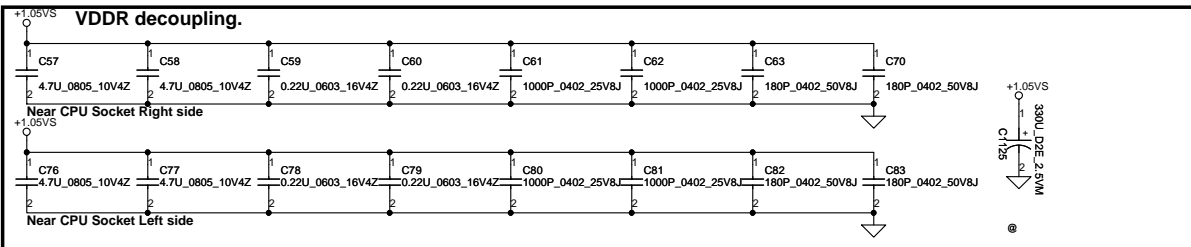
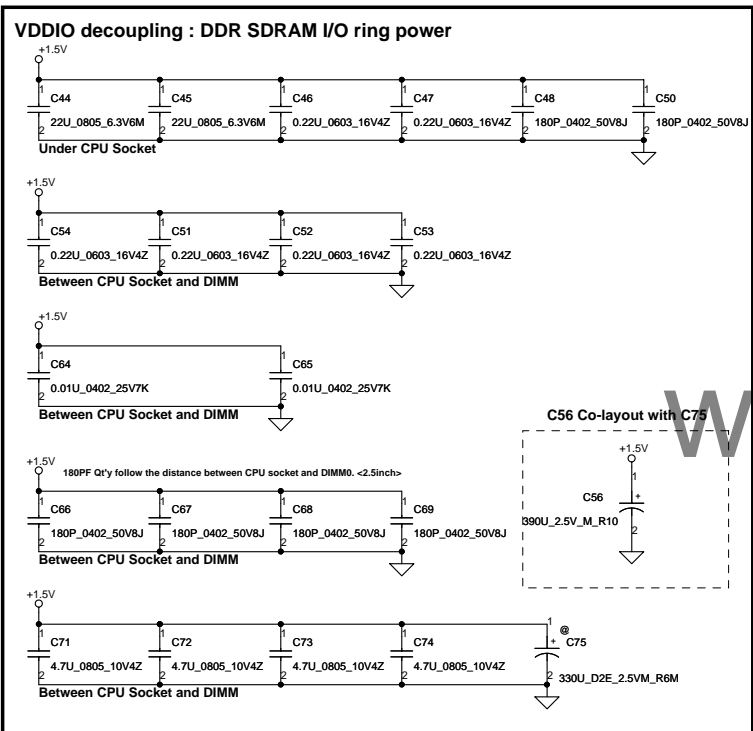
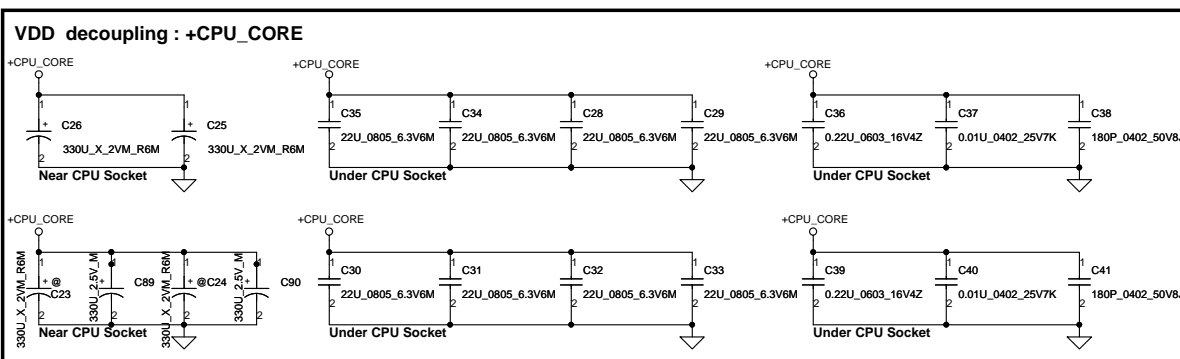


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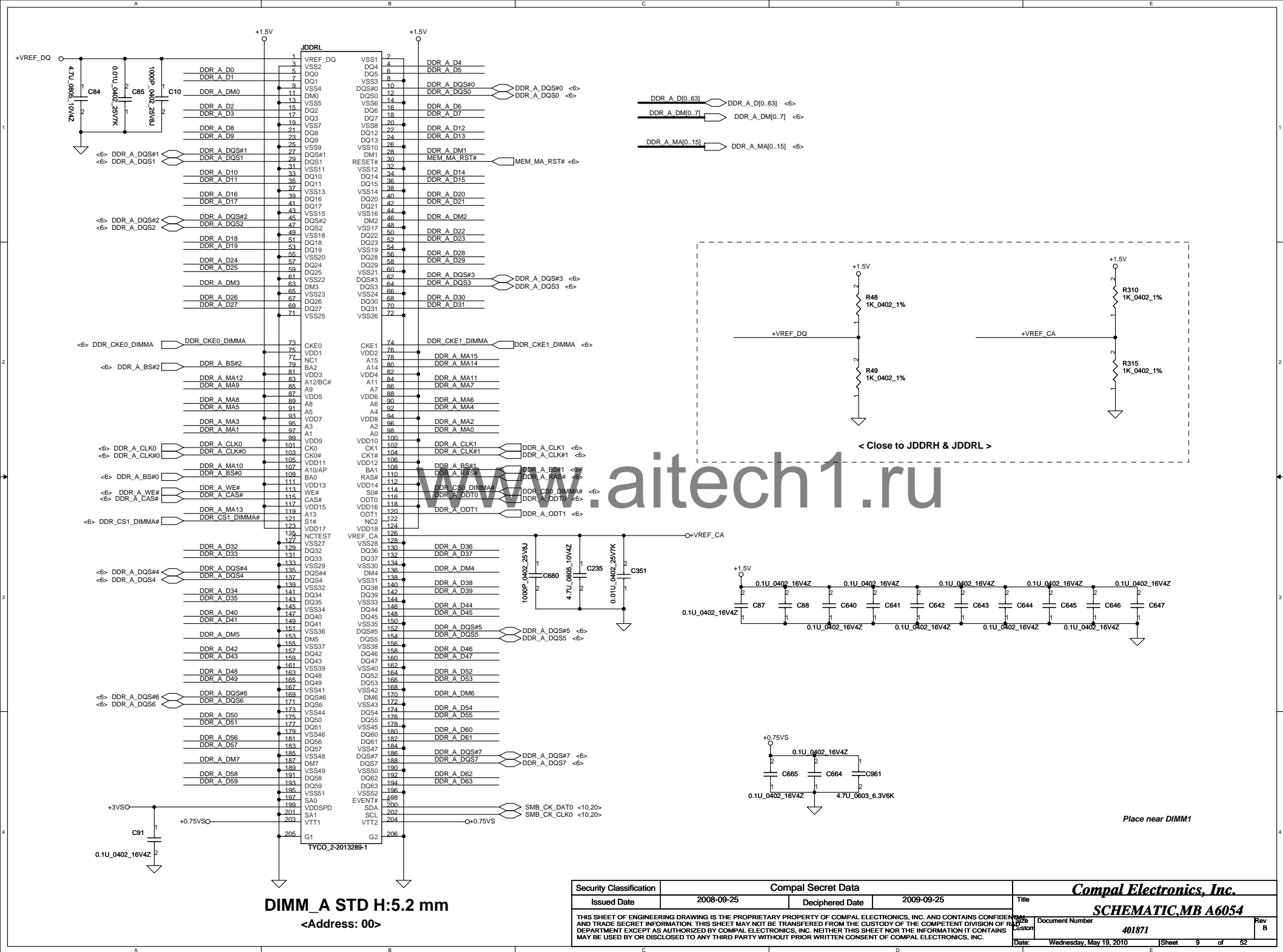


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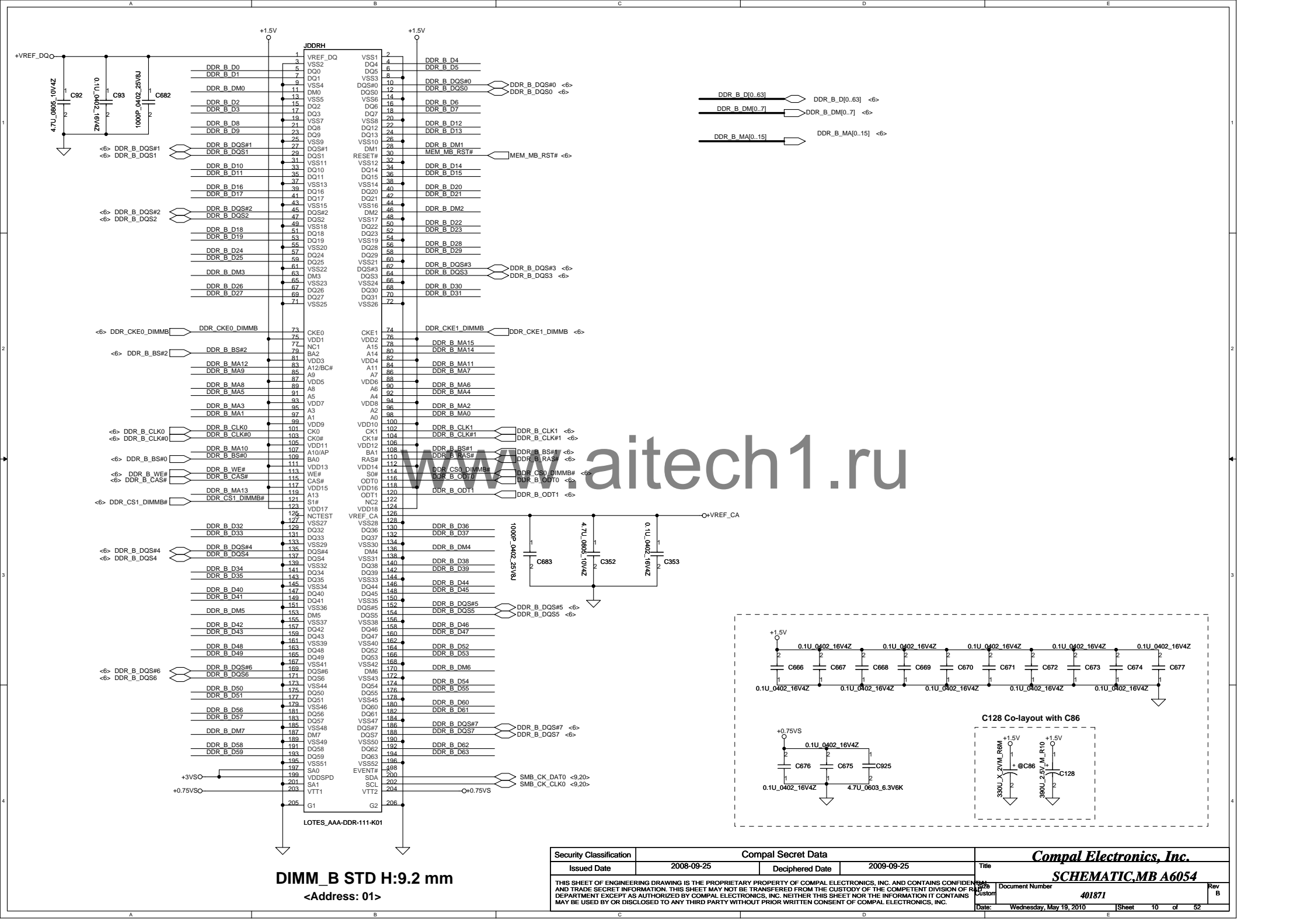
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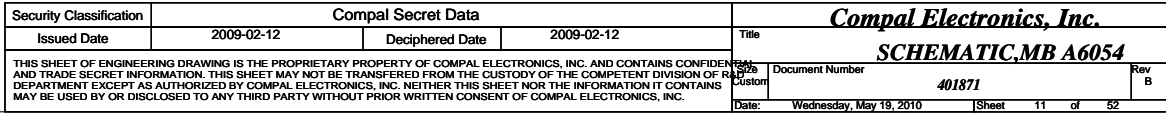


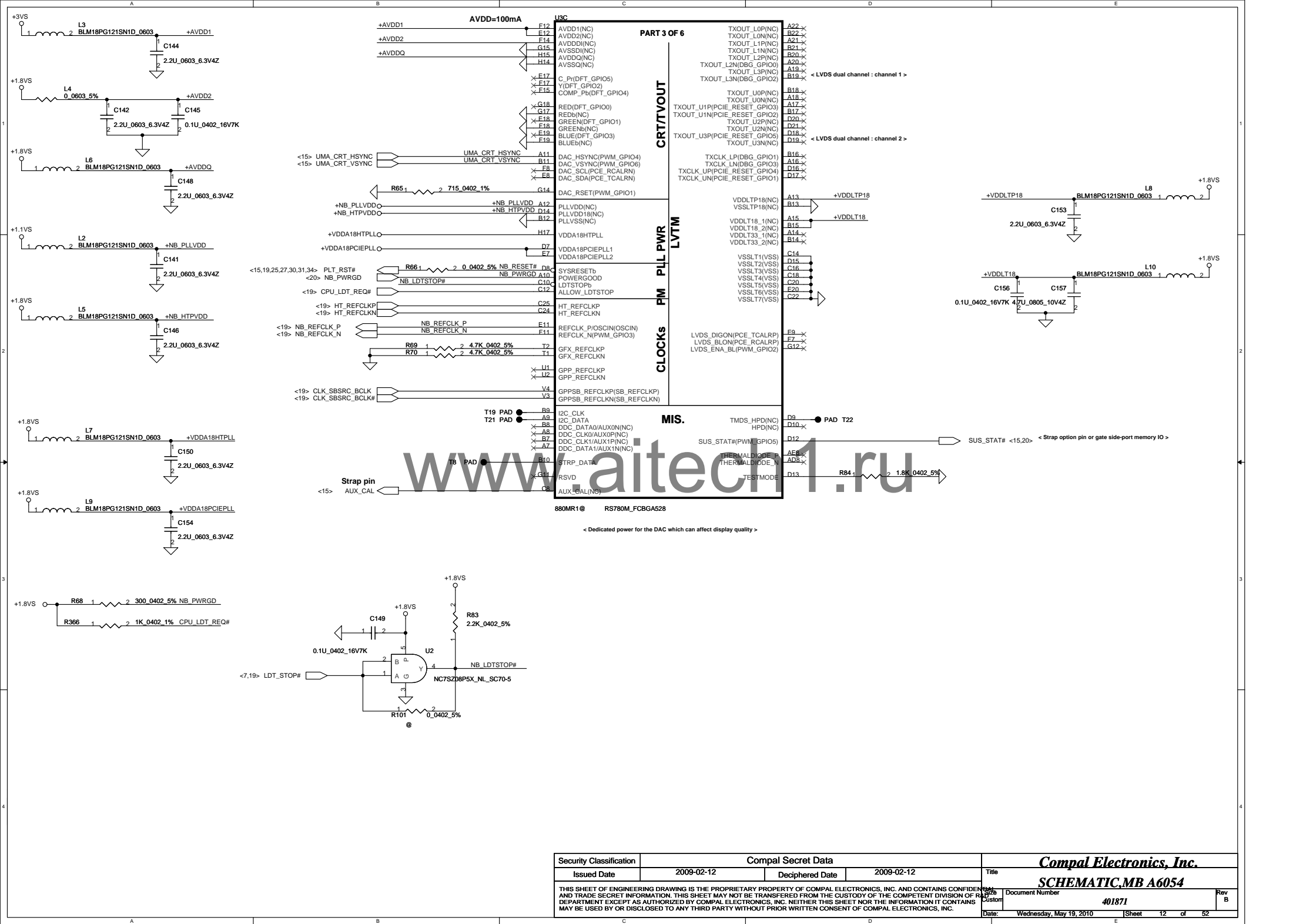
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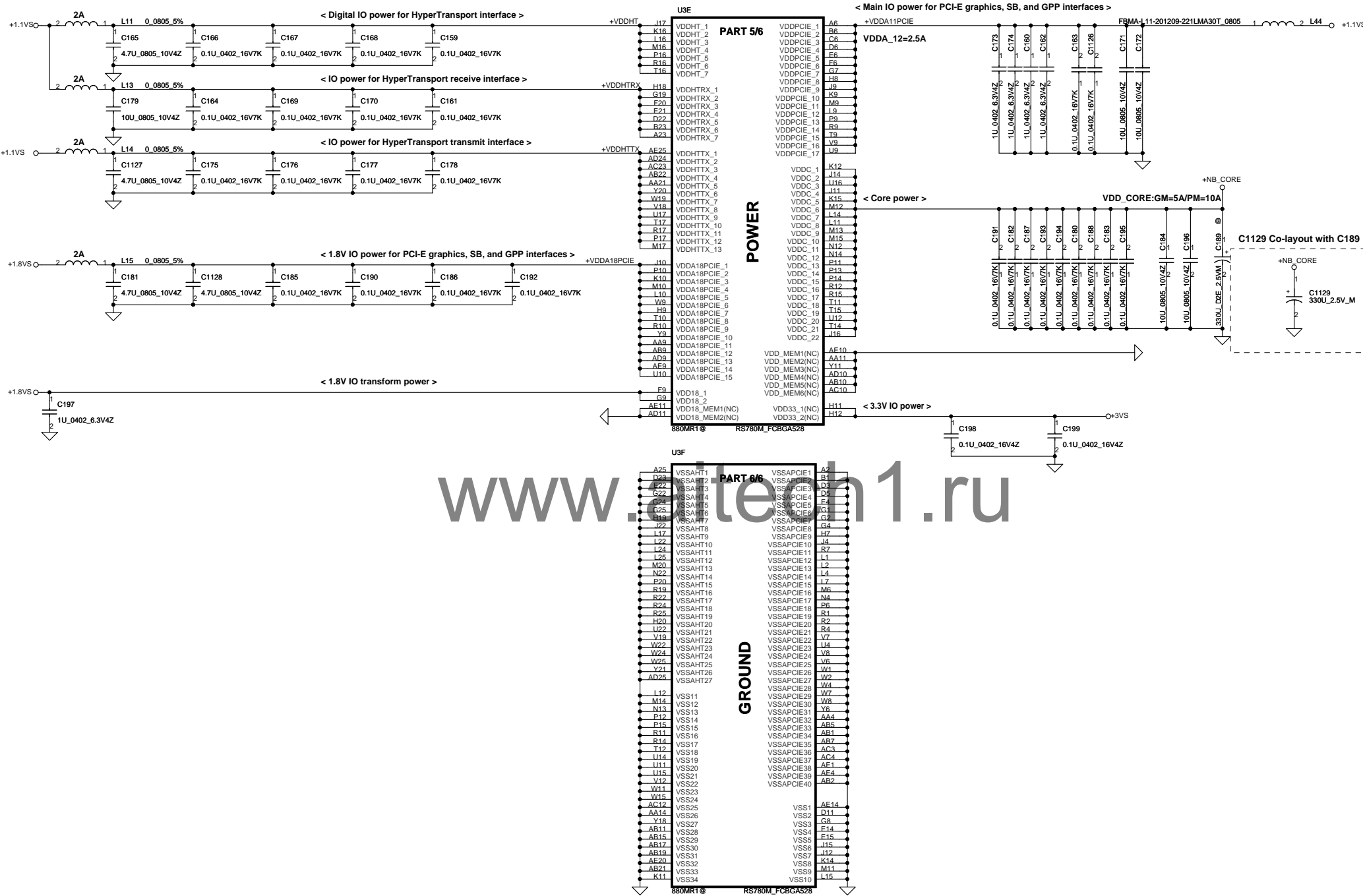


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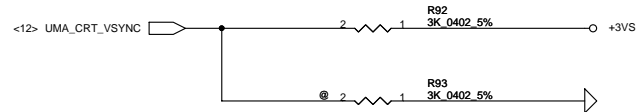






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< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Disable (RX881, RS880)
0 : Enable (RX881, RS880)

PIN: RS880--> VSYNC#

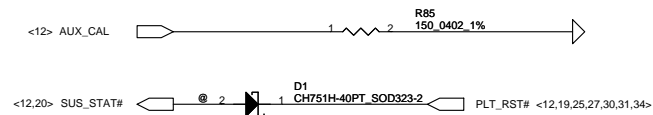
< RS880 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



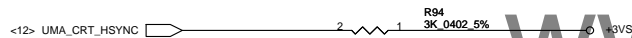
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

1: Disable (Can still be enabled using nbcfg register access)
0: Enable

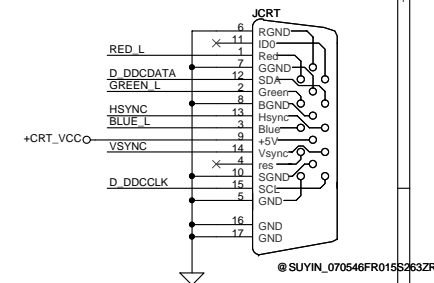
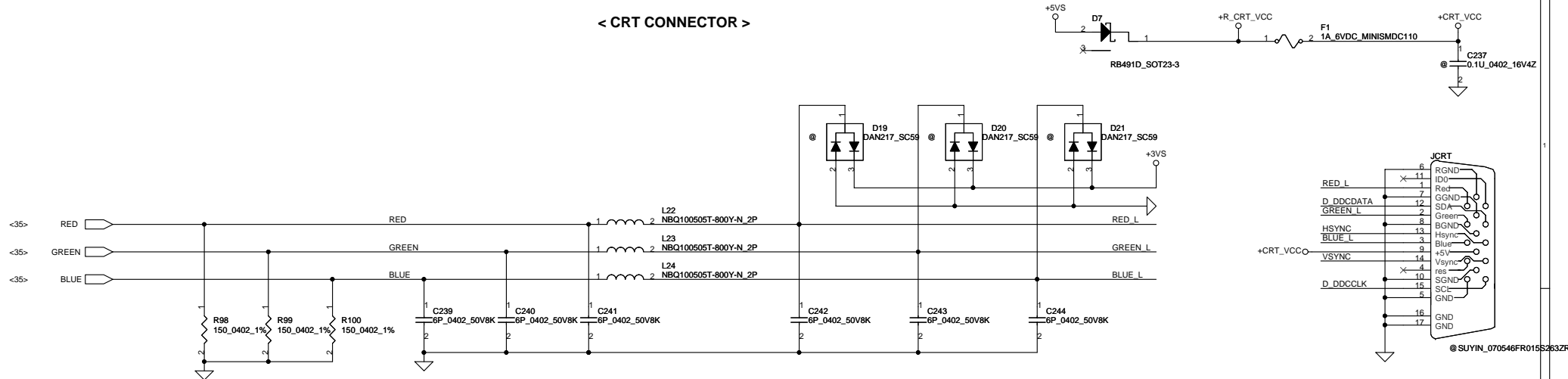
RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

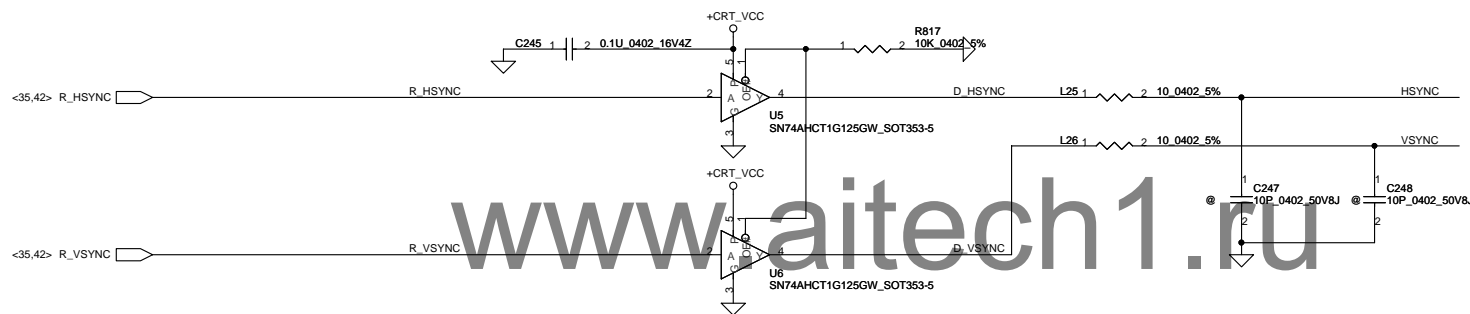
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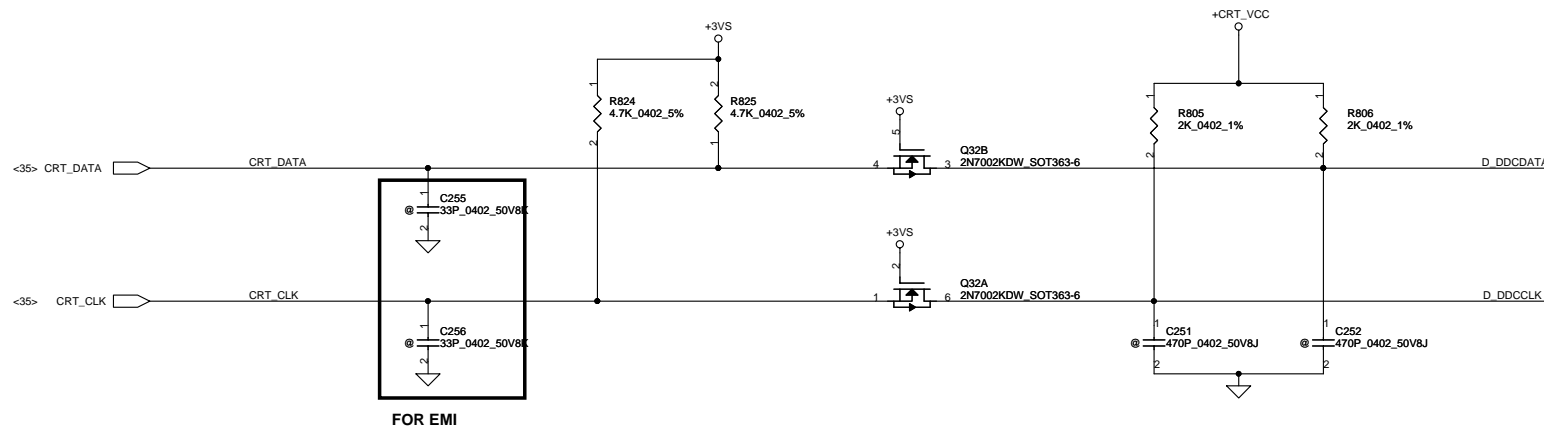
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< SYNC SIGNAL >



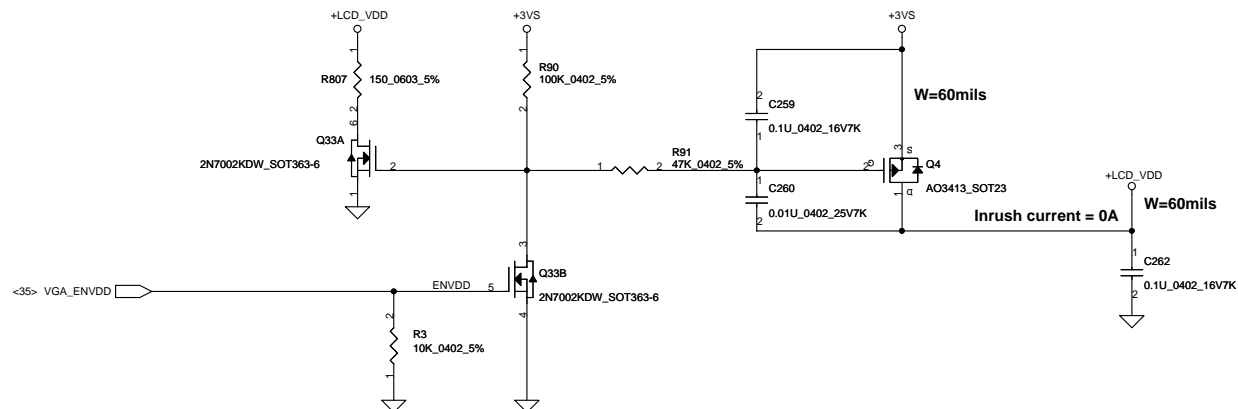
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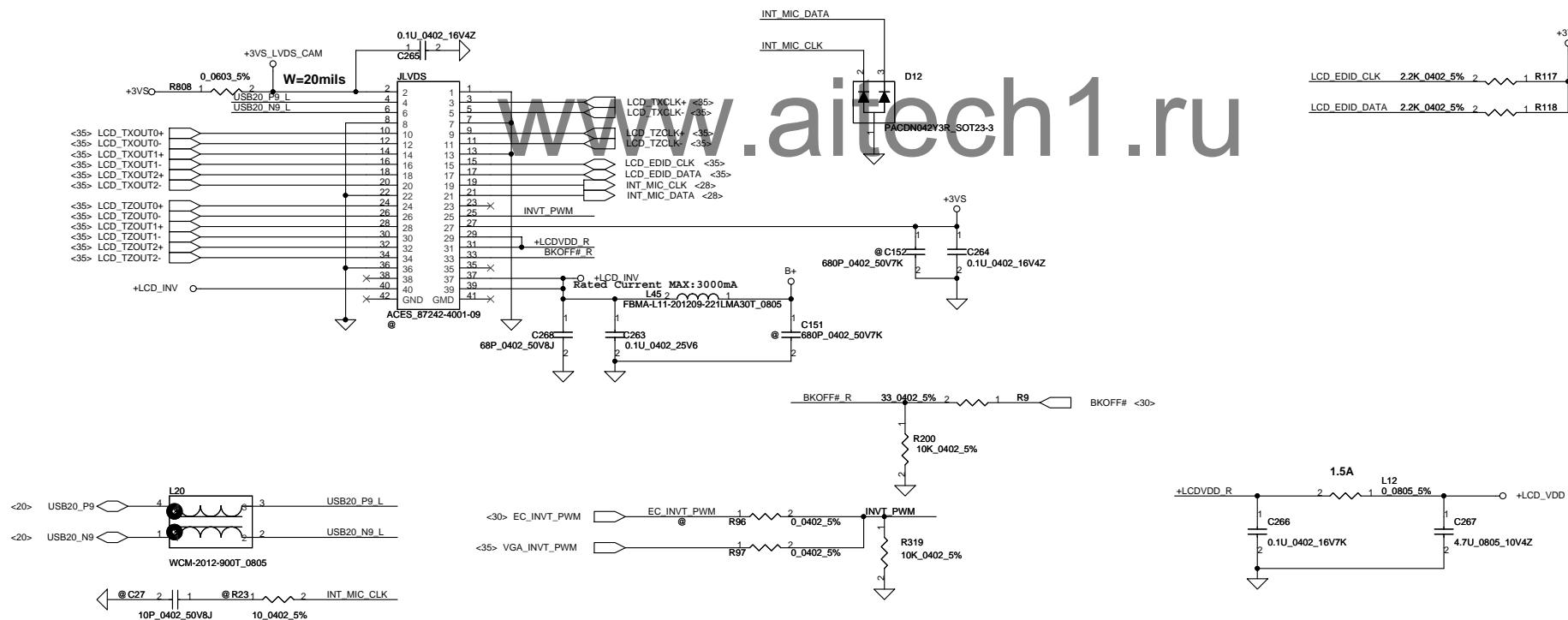
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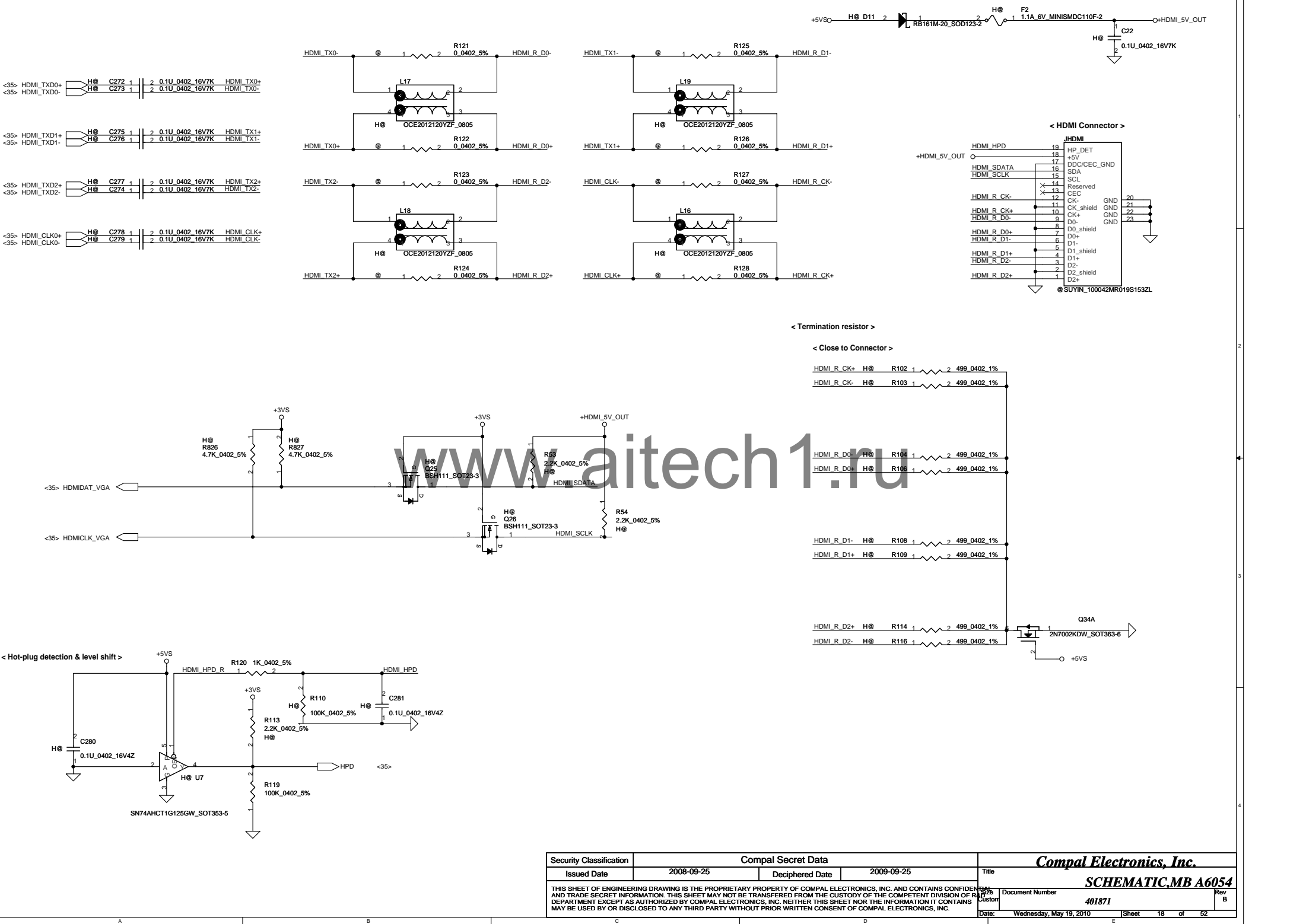
LCD/PANEL BD. Conn.



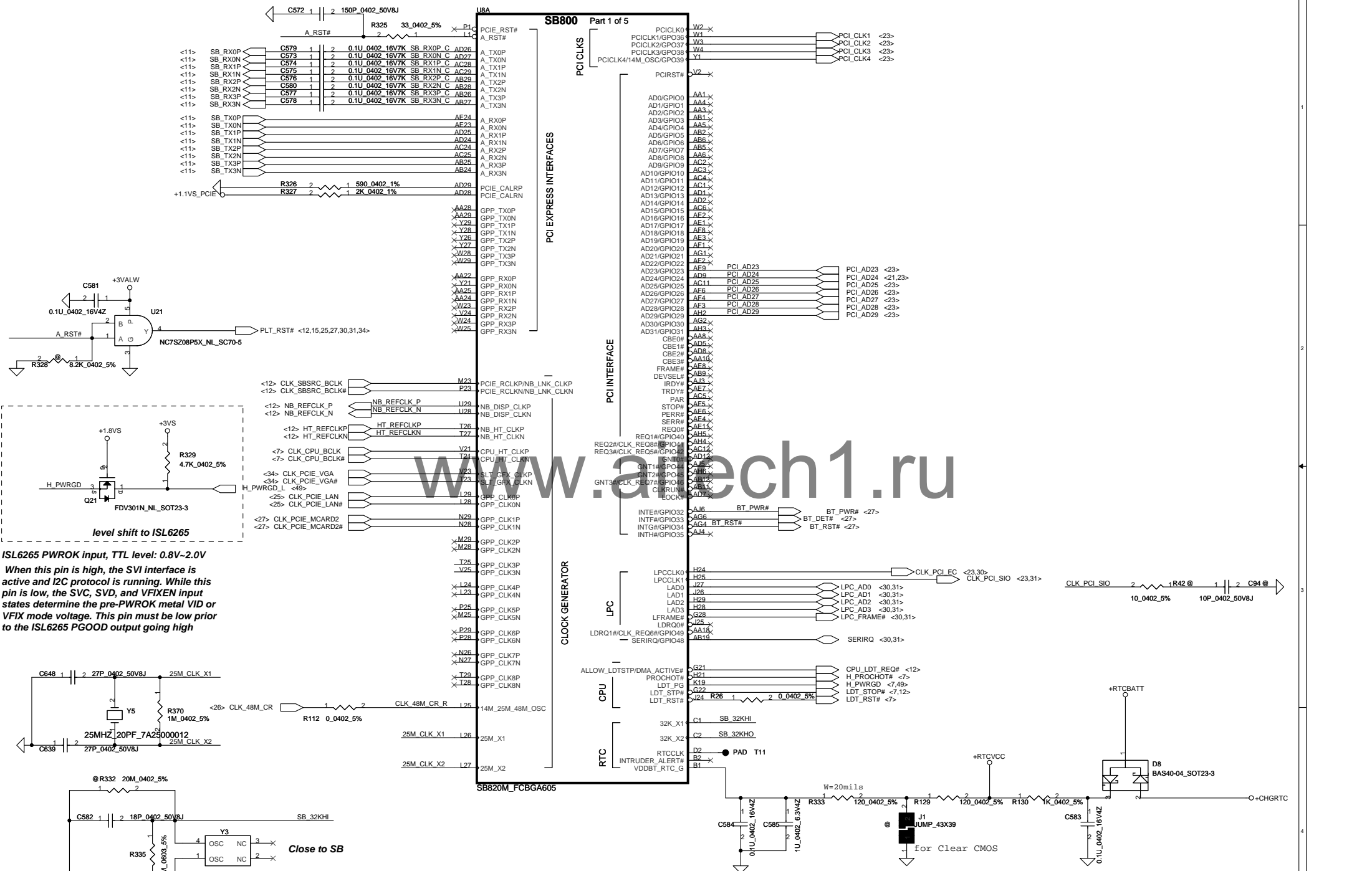
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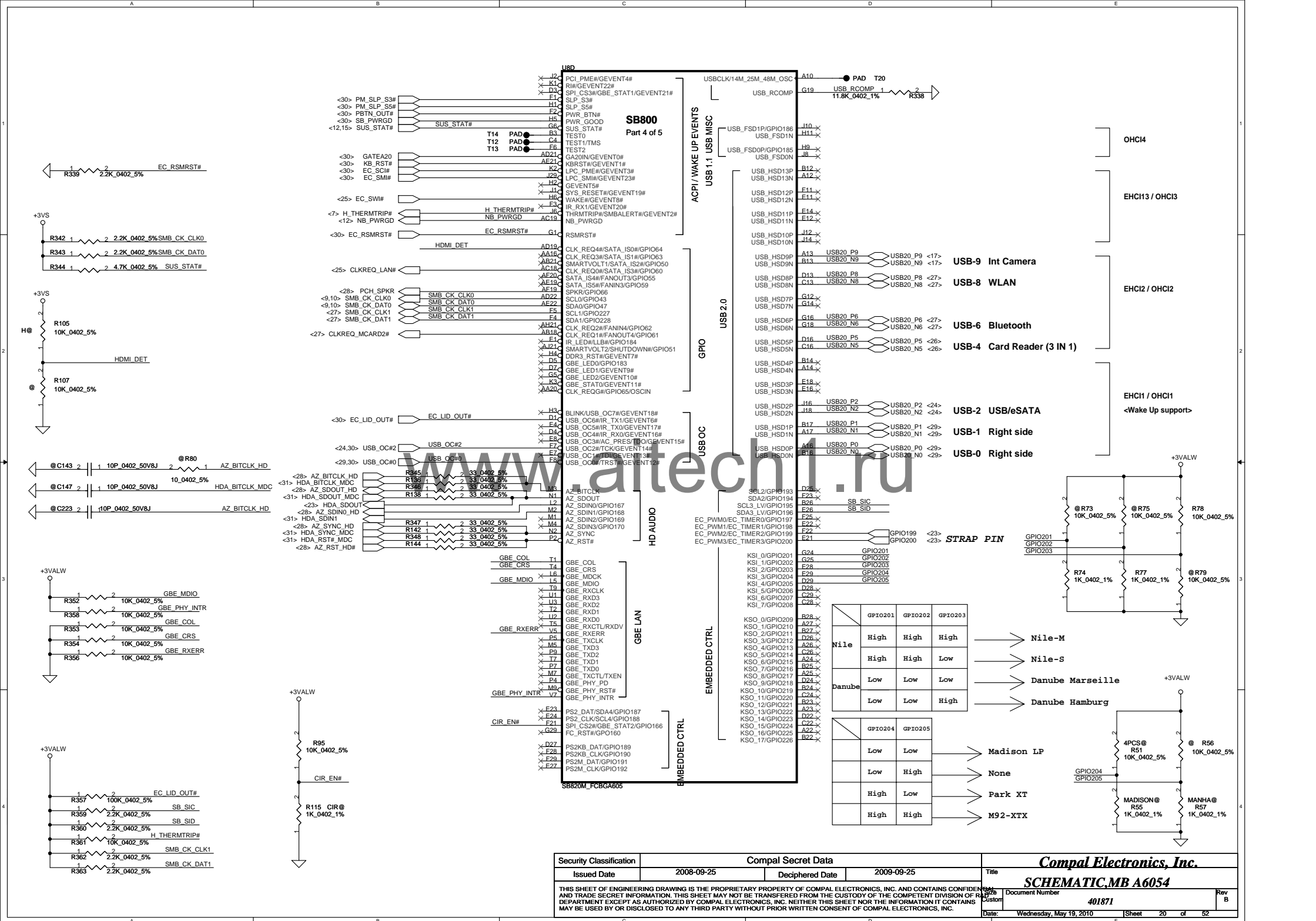


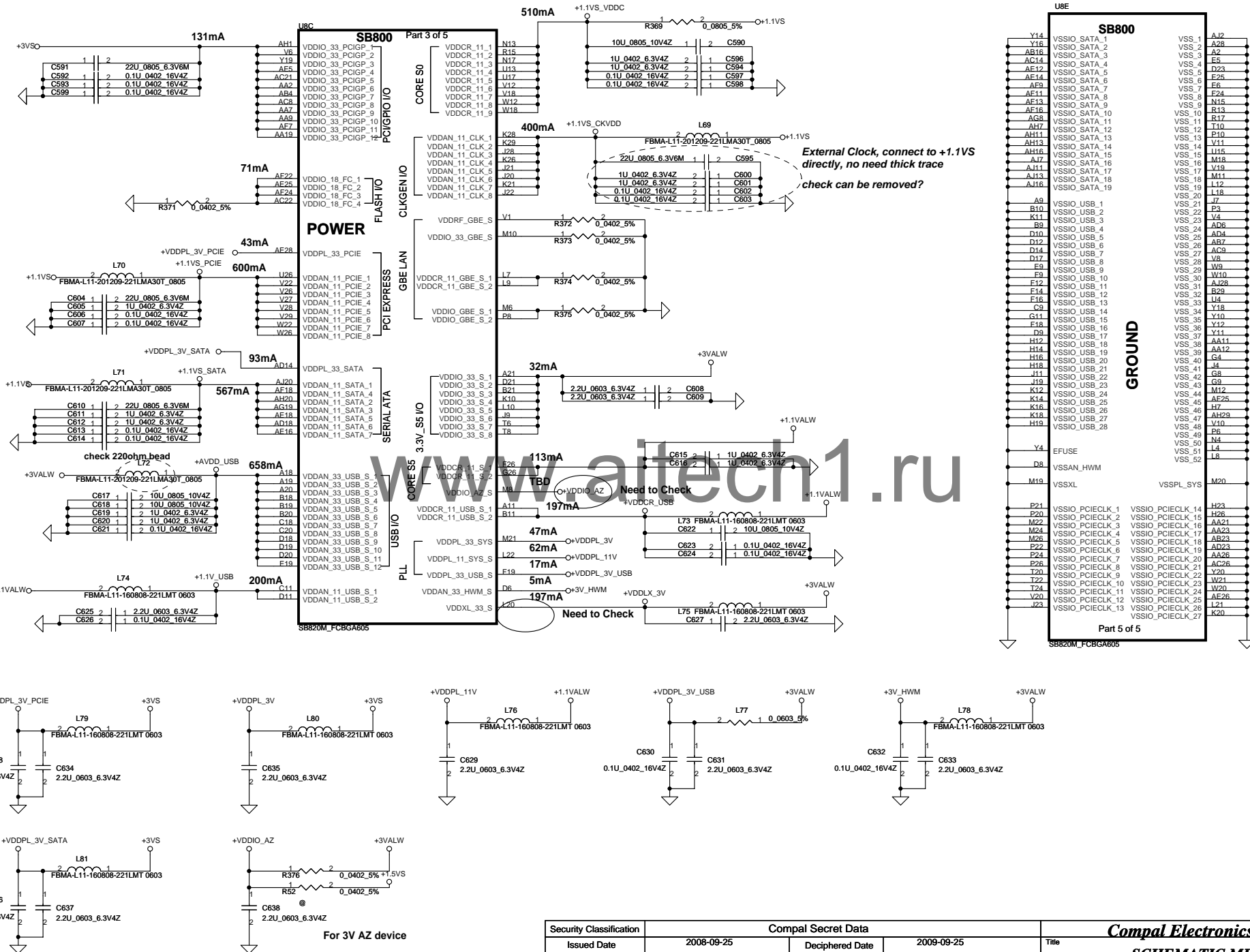
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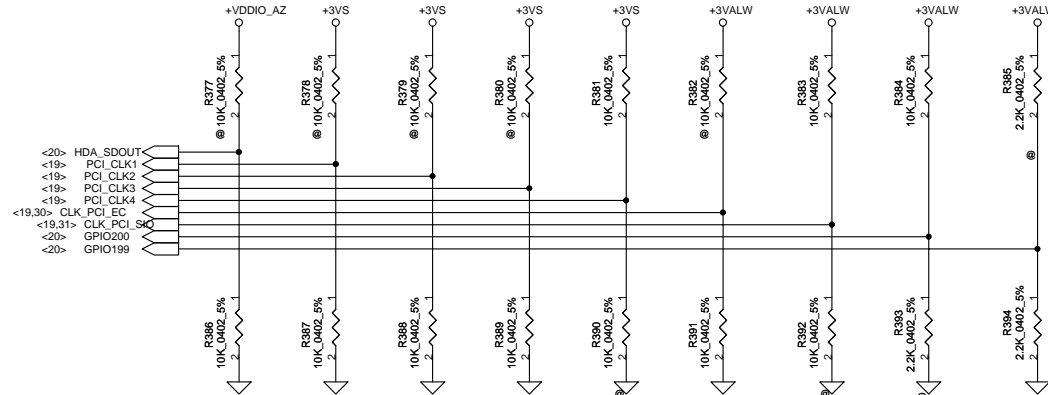




REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT		H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE		L,L = LPC ROM L,L = FWH ROM	



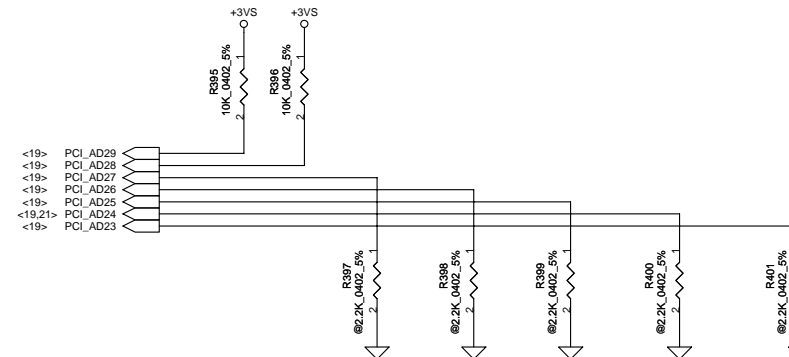
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

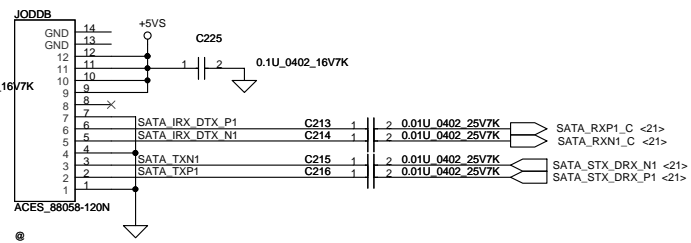
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default

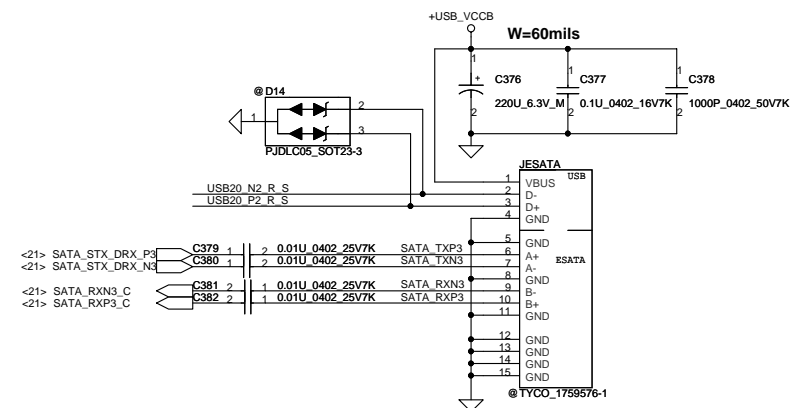
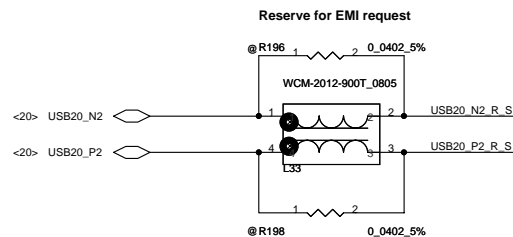


< SATA ODD Conn >

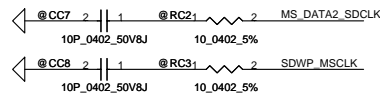
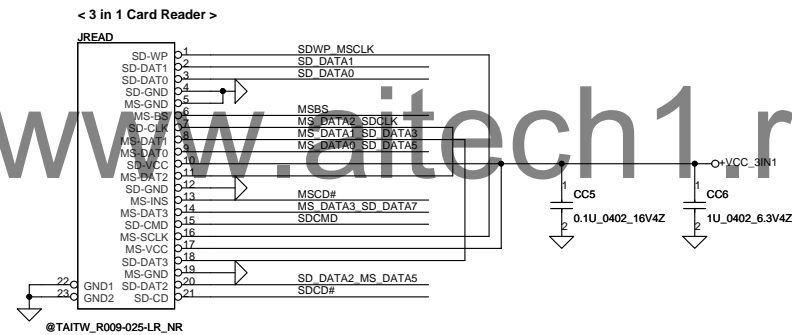
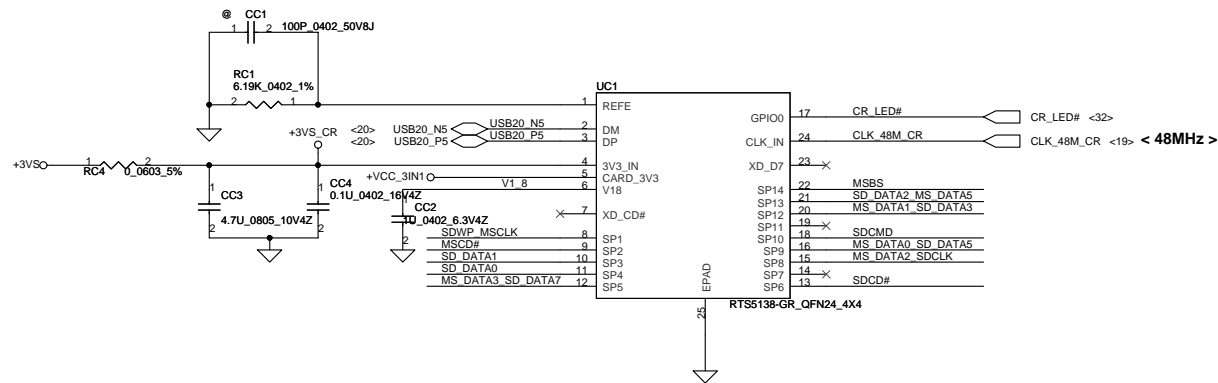


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Timing diagram for the USB to RS-485 module. The diagram shows the relationship between the USB_VCCB, +5VALWO, USB_EN#, and USB_OC# signals. The module is labeled '2A' and 'W=60mils'. The diagram includes a 4.7uF capacitor and a 10V4Z diode. The USB_EN# signal is shown as a pulse, and the USB_OC# signal is shown as a pulse. The timing is labeled with 'U11' and 'S08'.

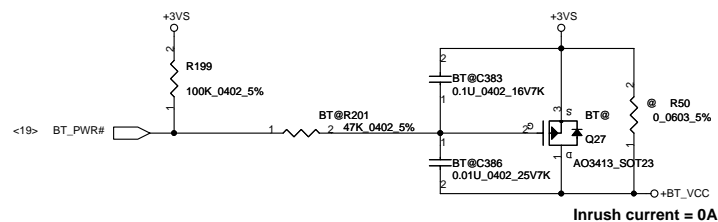


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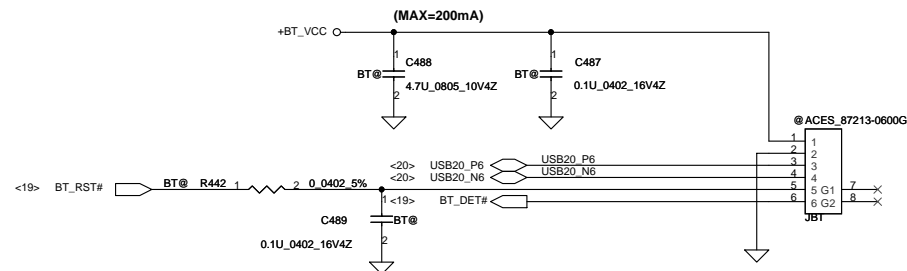


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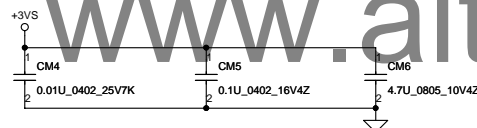
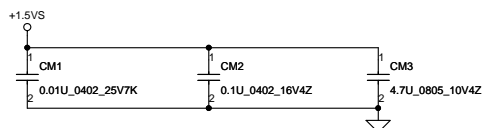
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< Bluetooth Connector >

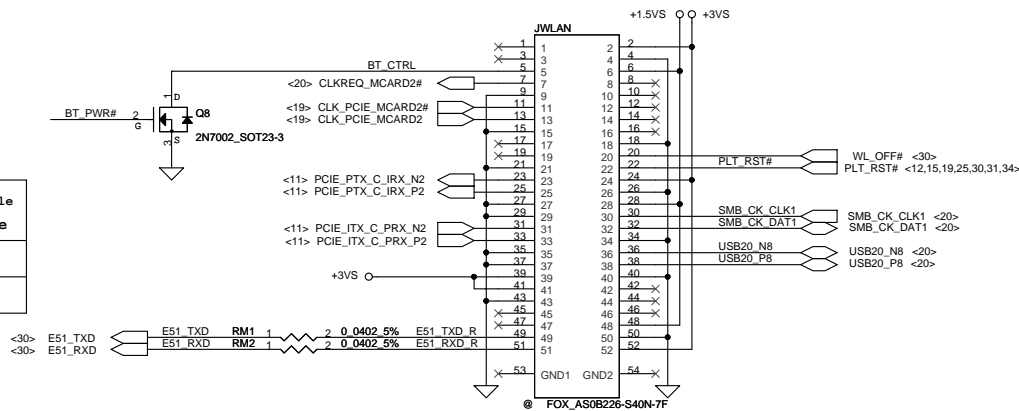


< PCIe Mini Card for WLAN >



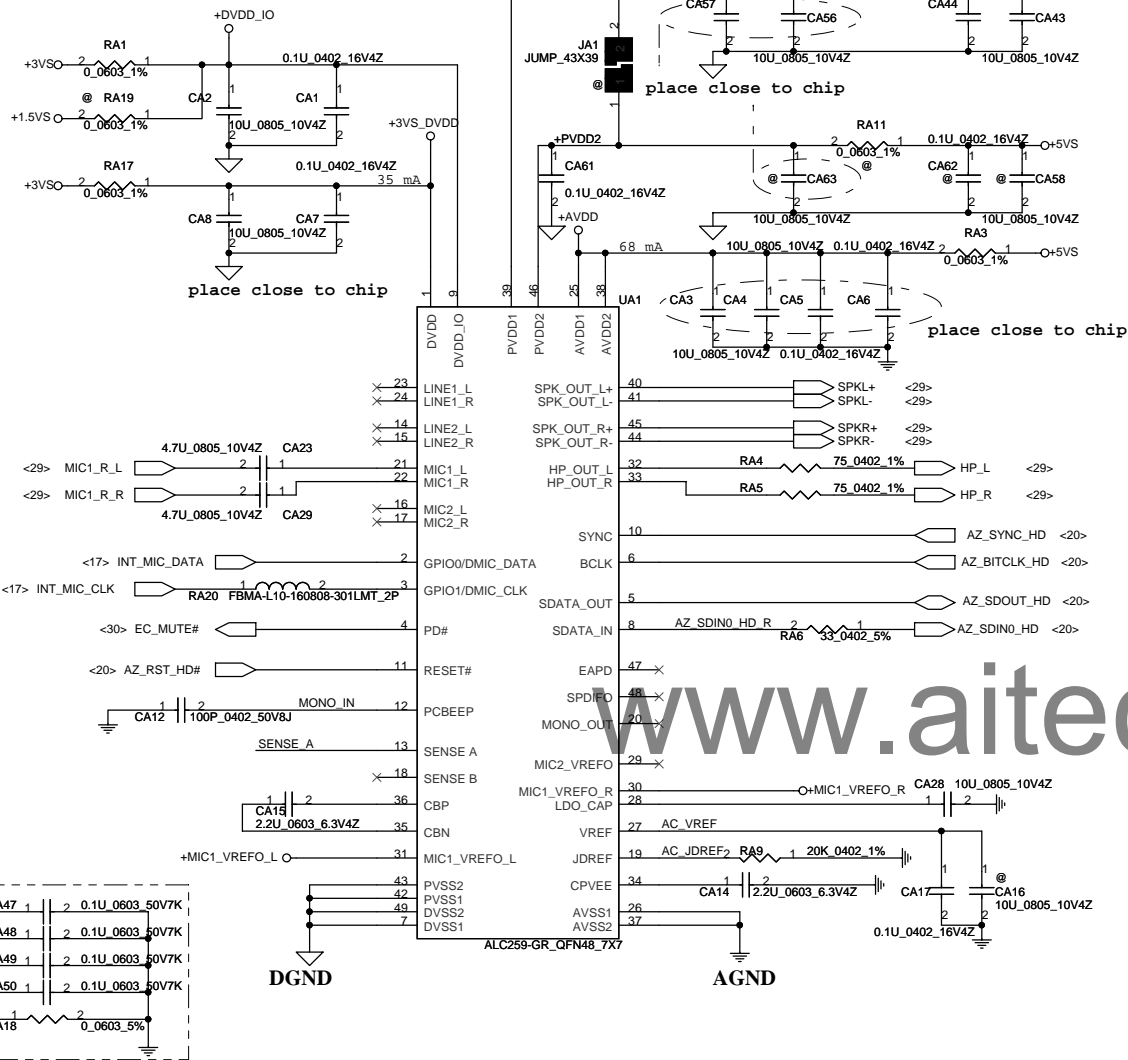
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	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

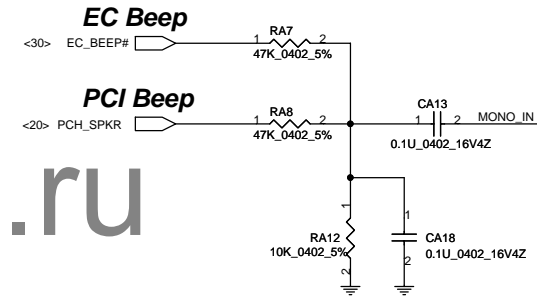


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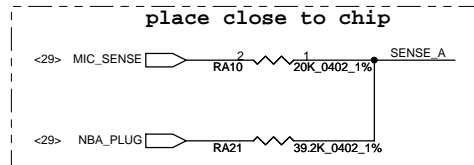
Codec



Beep sound

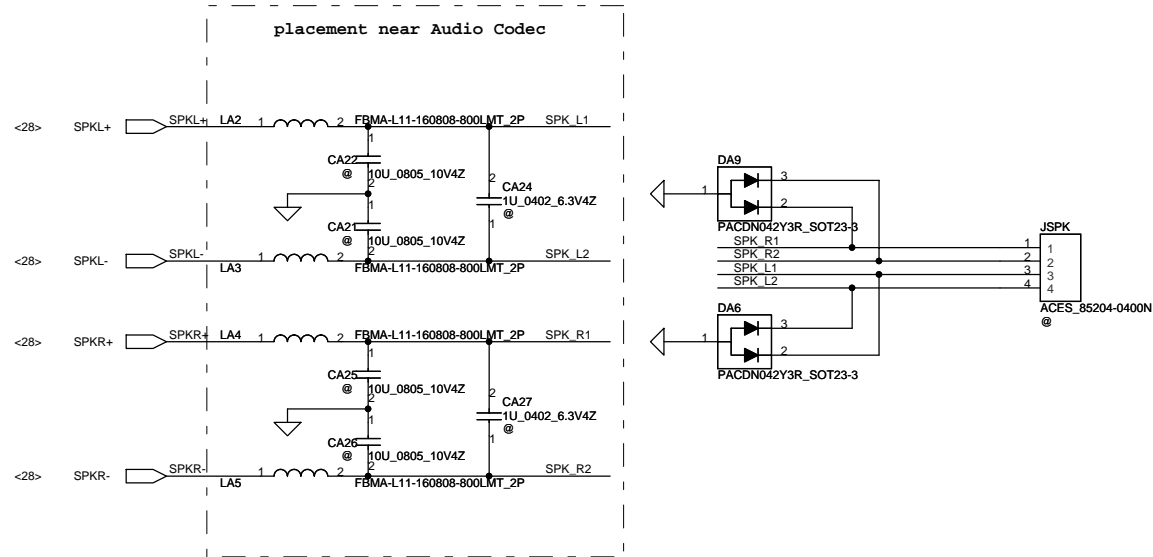


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



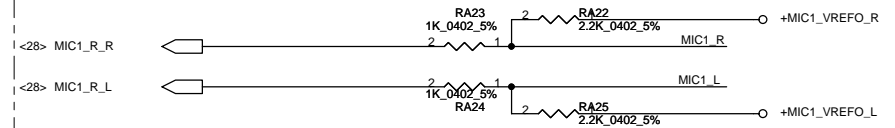
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	SCHEMATIC, MB A6054
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Speaker Connector



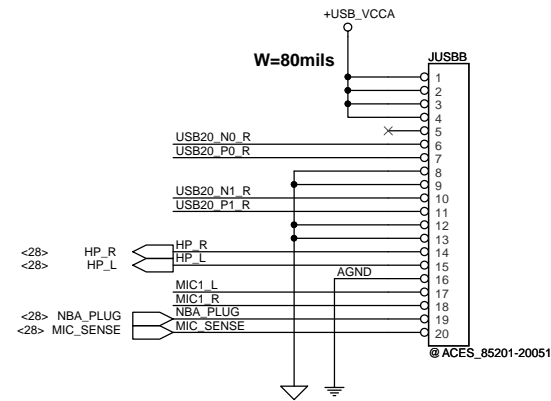
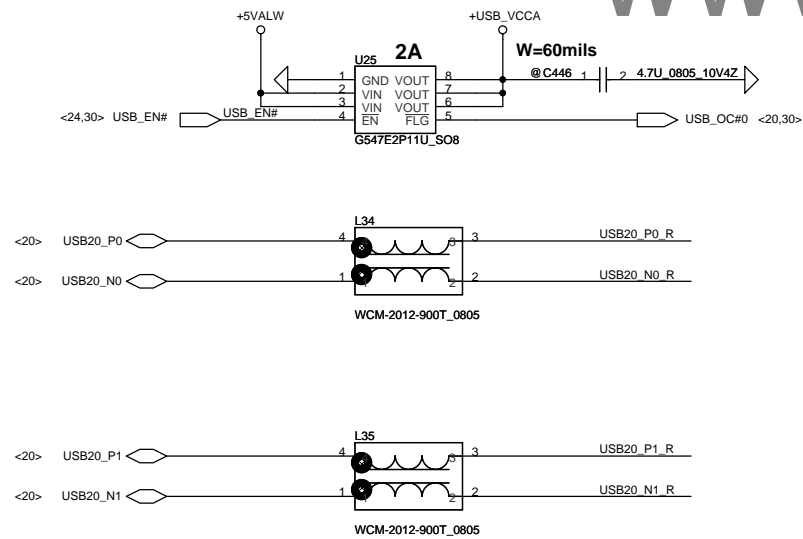
HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK

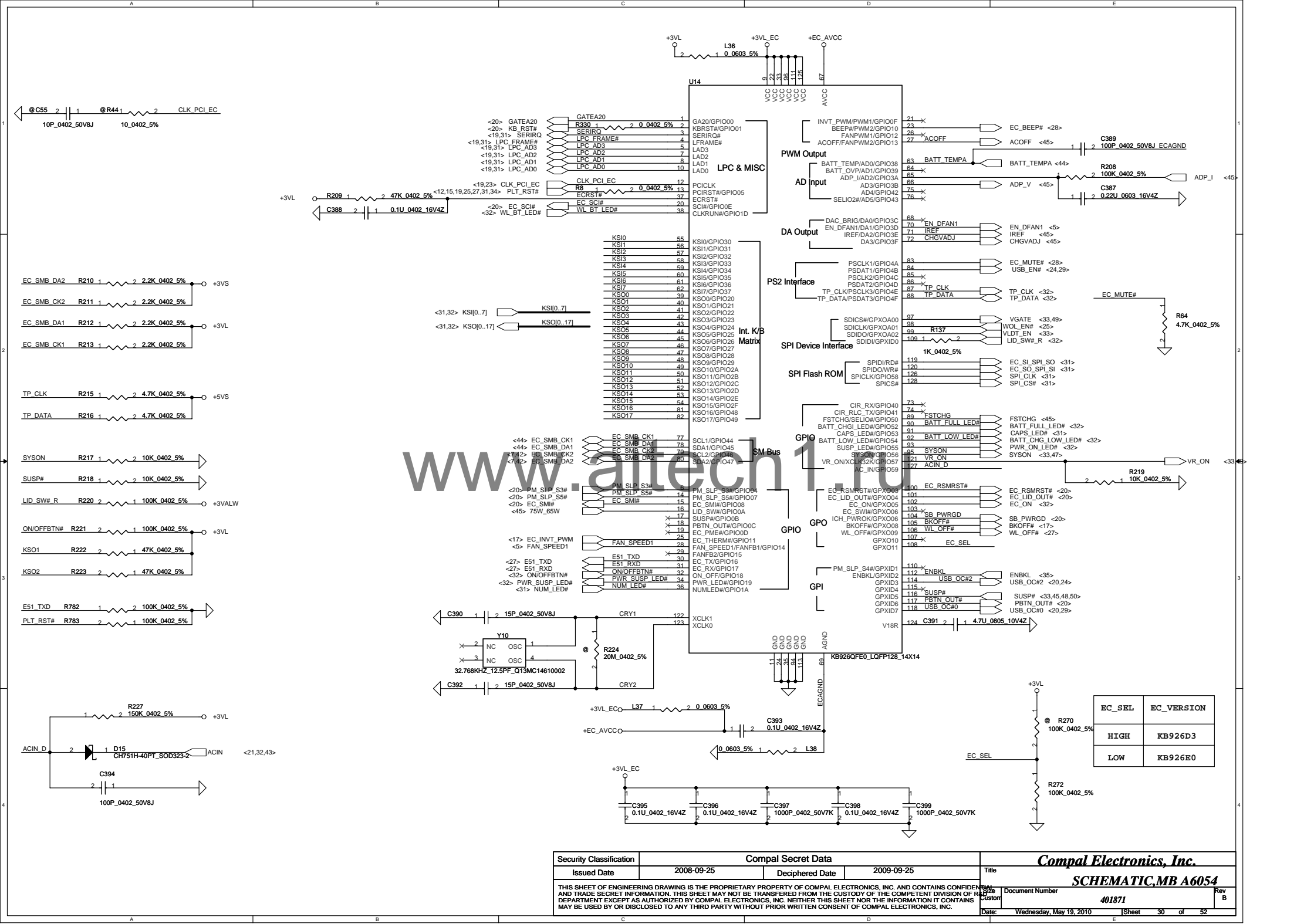


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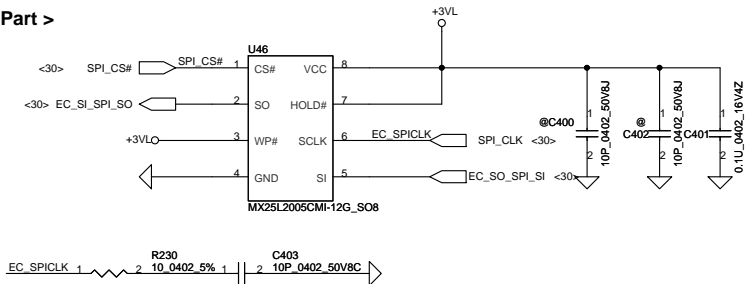
Audio & USB Sub-Board Conn.



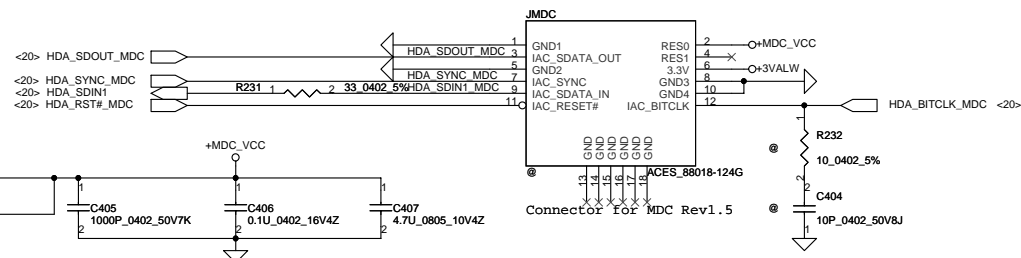
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< ROM Part >

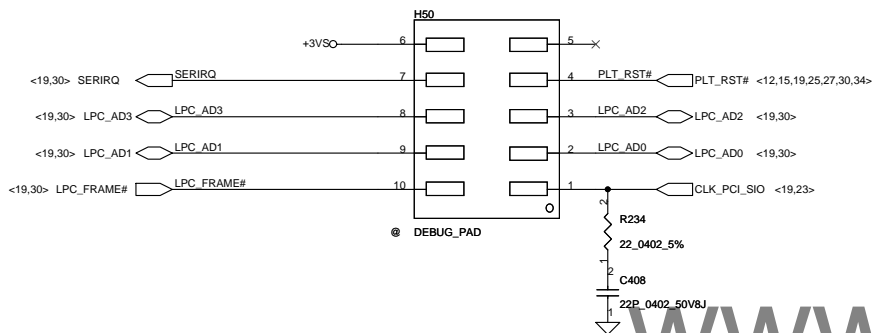


< MDC 1.5 Conn >

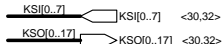


< LPC Debug Port >

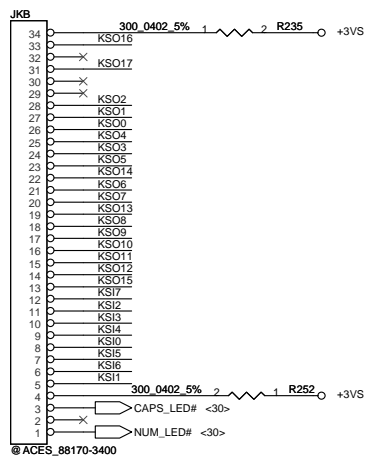
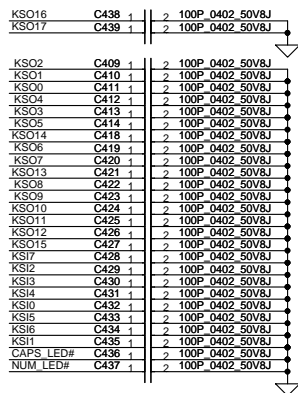
Please place the PAD under DDR DIMM.



< KEYBOARD Conn >

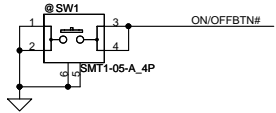


< For EMI >

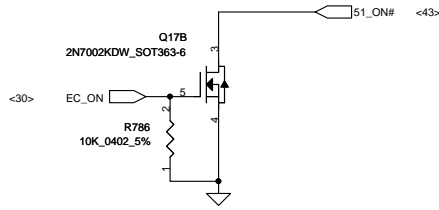


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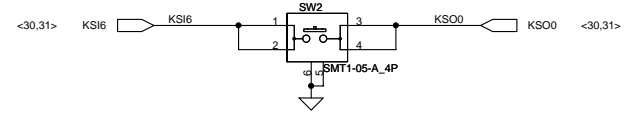
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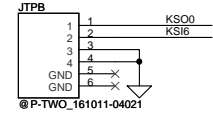
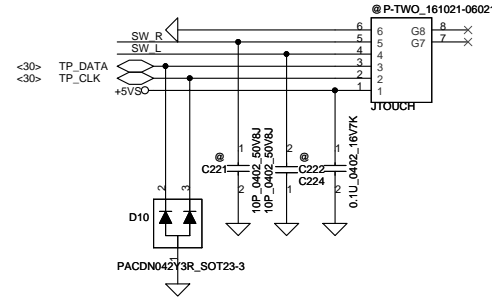
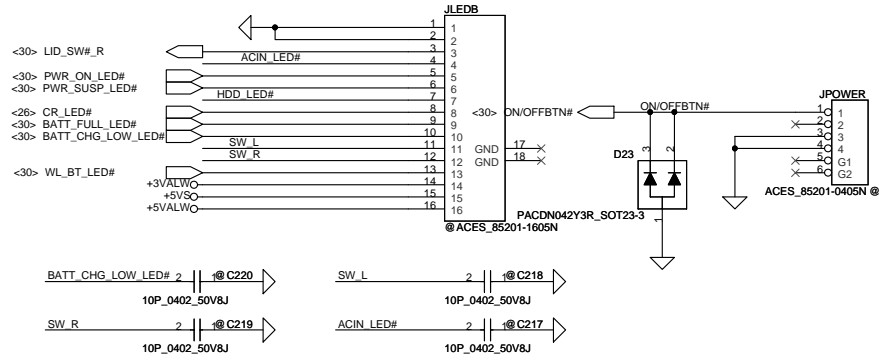
< Power Button Circuit >



< TP on & off BTN on M/B>

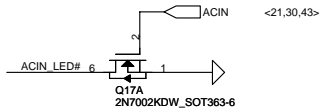


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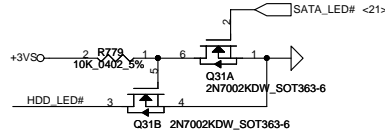


LED Circuit

DC-IN LED

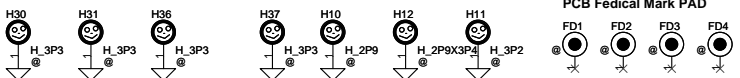
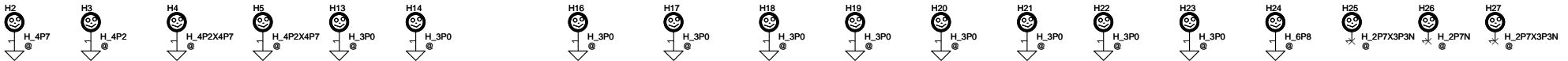


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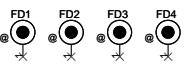


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SCREW

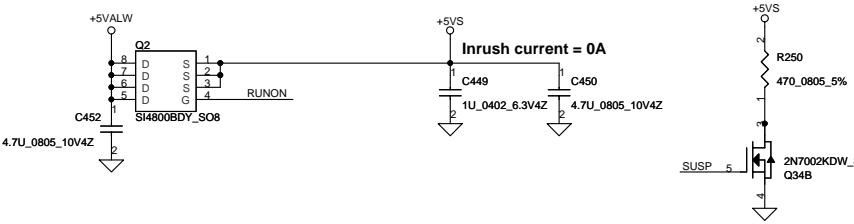


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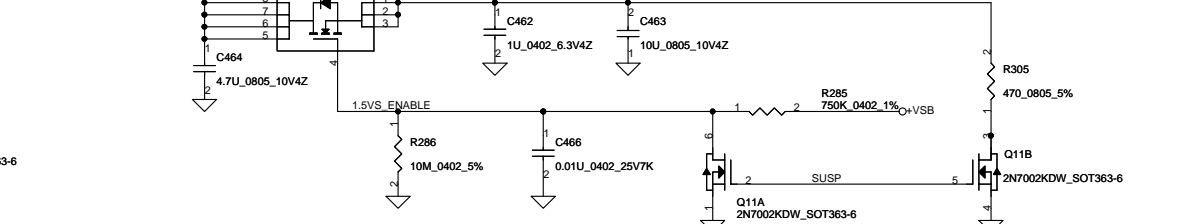


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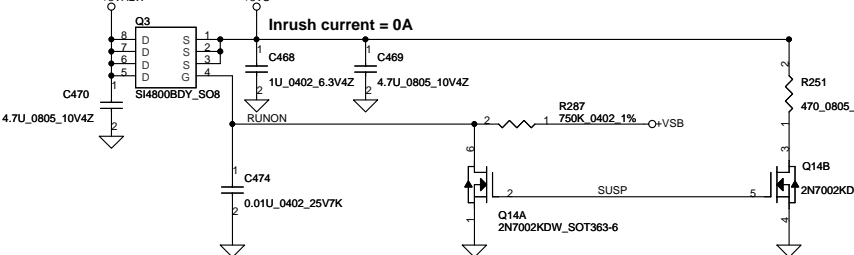
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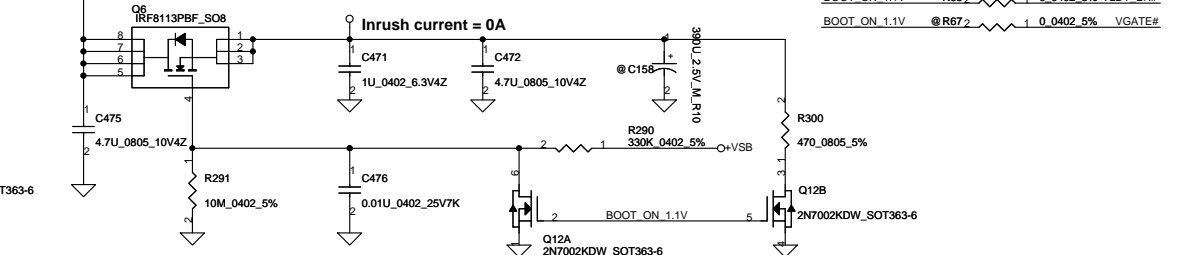
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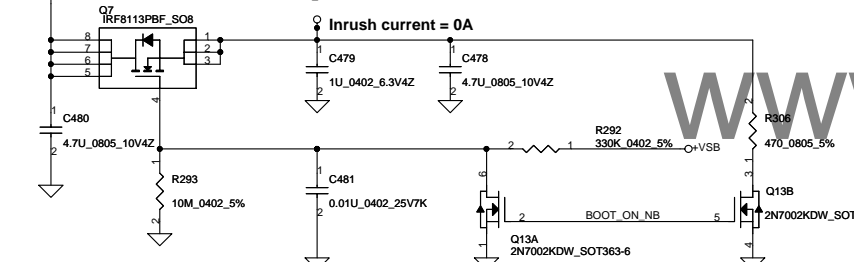
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< +1.1VALW TO +1.1VS >



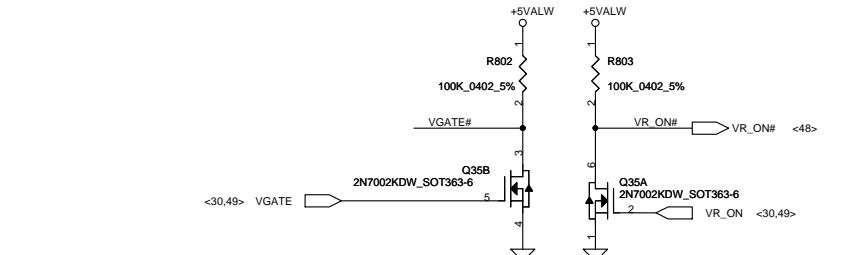
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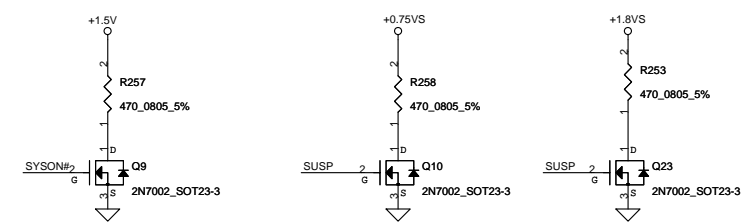
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



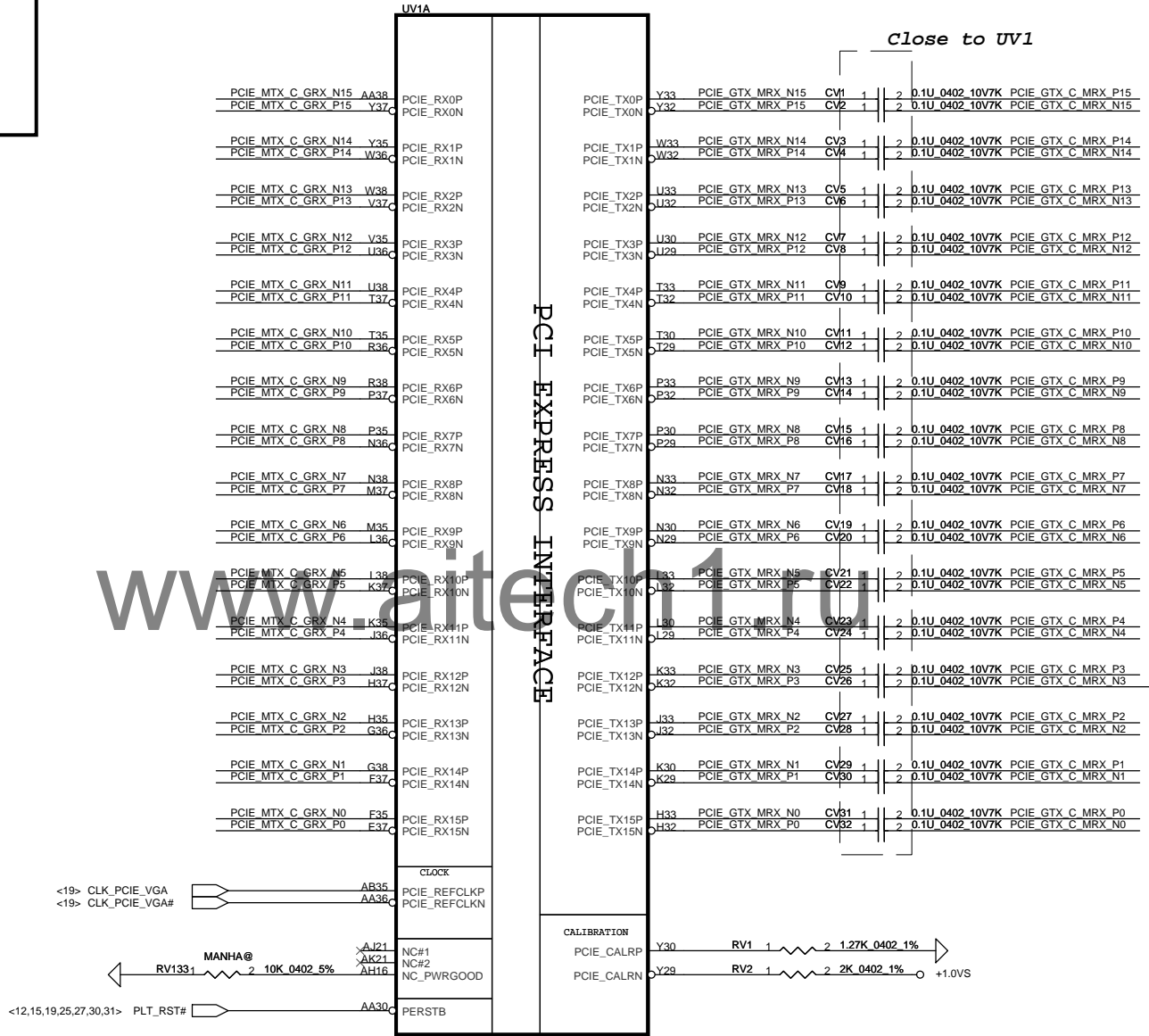
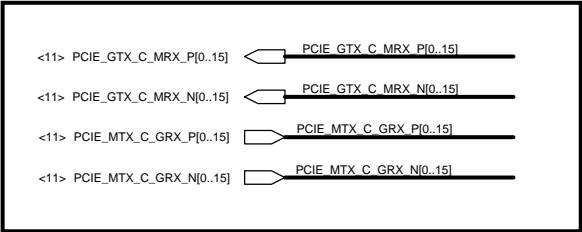
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BOOT_ON_NB R46 1 0.0402_5% VLDT_EN#
BOOT_ON_NB @R47 1 0.0402_5% VGATE#



< Discharge circuit >



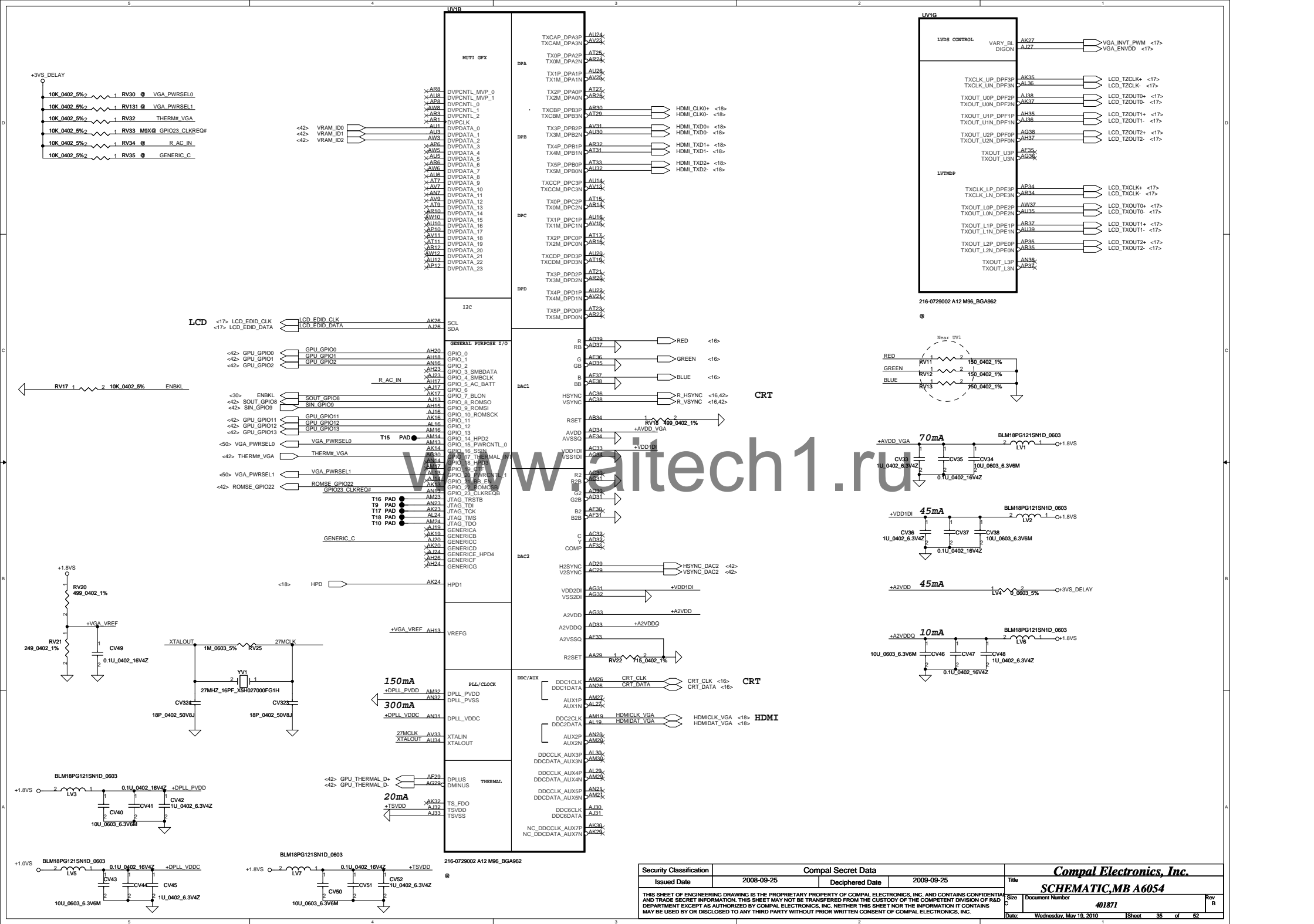
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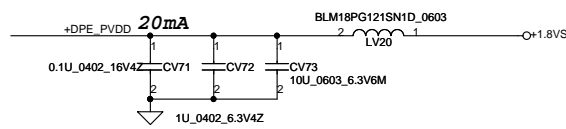
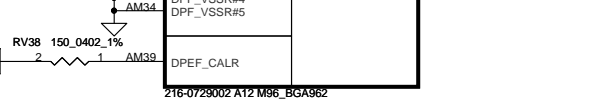
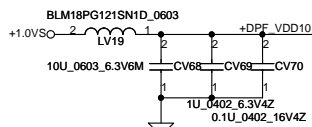


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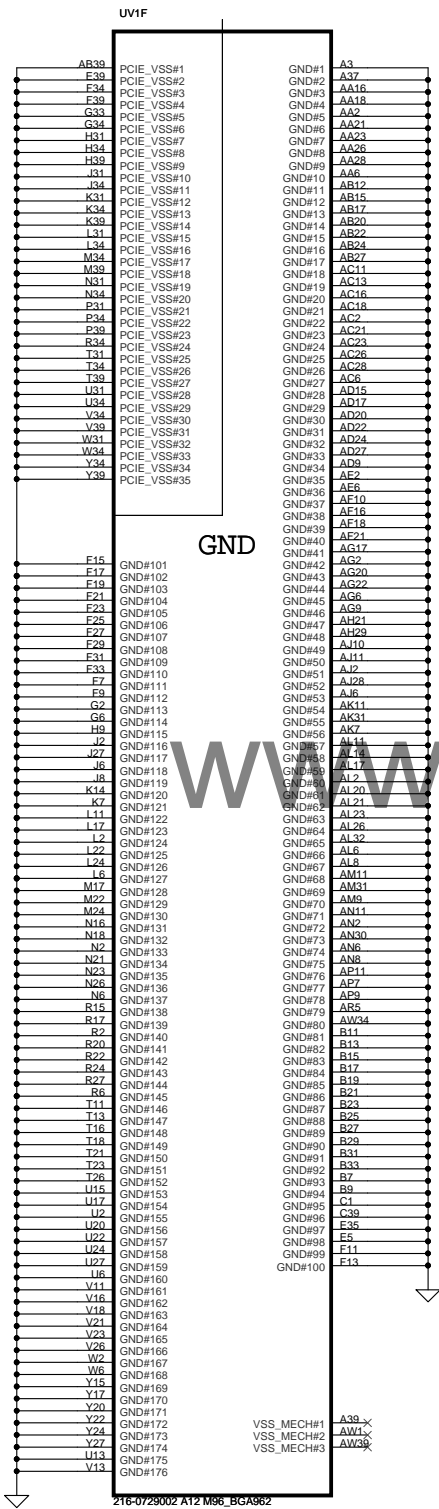
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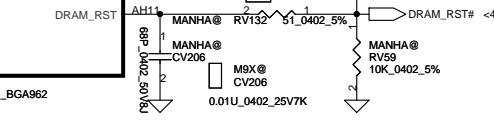
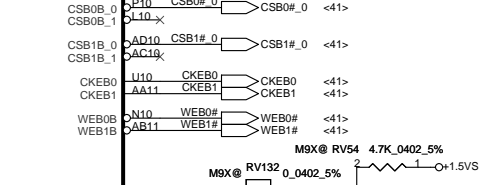
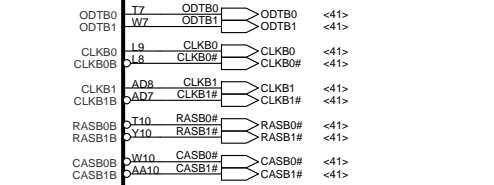
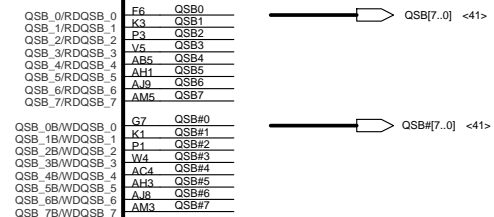
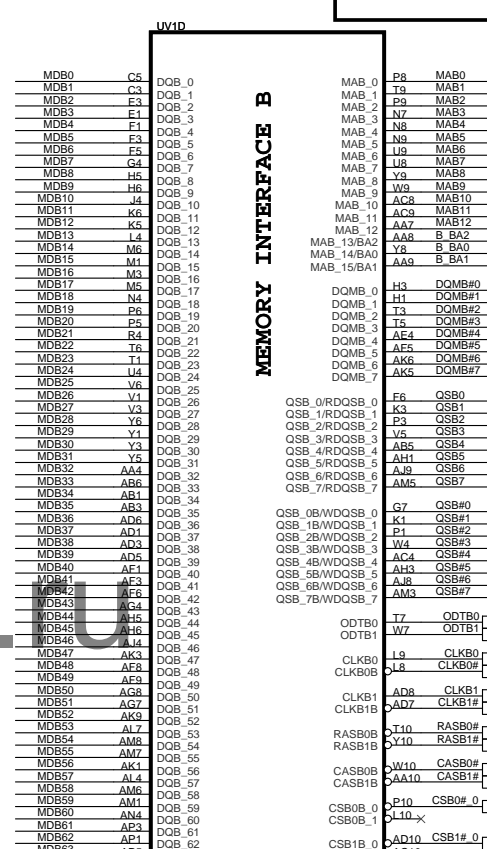
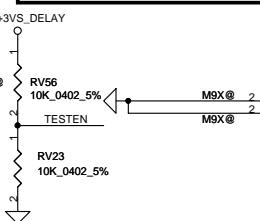
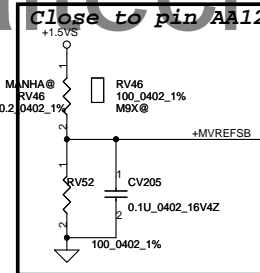
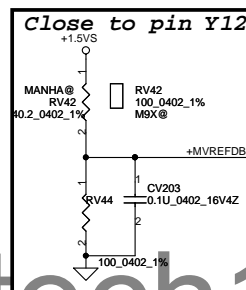
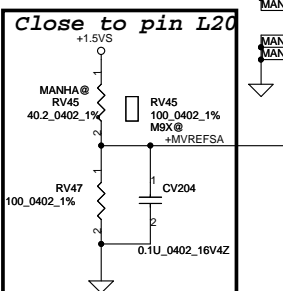
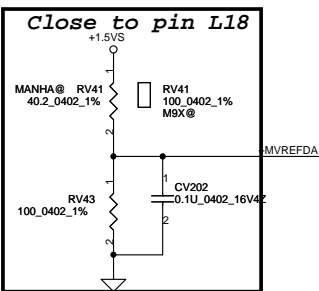
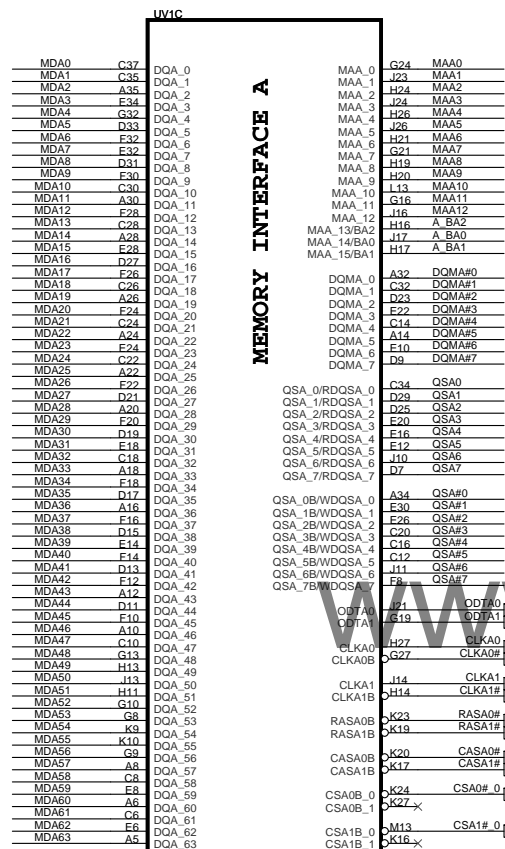
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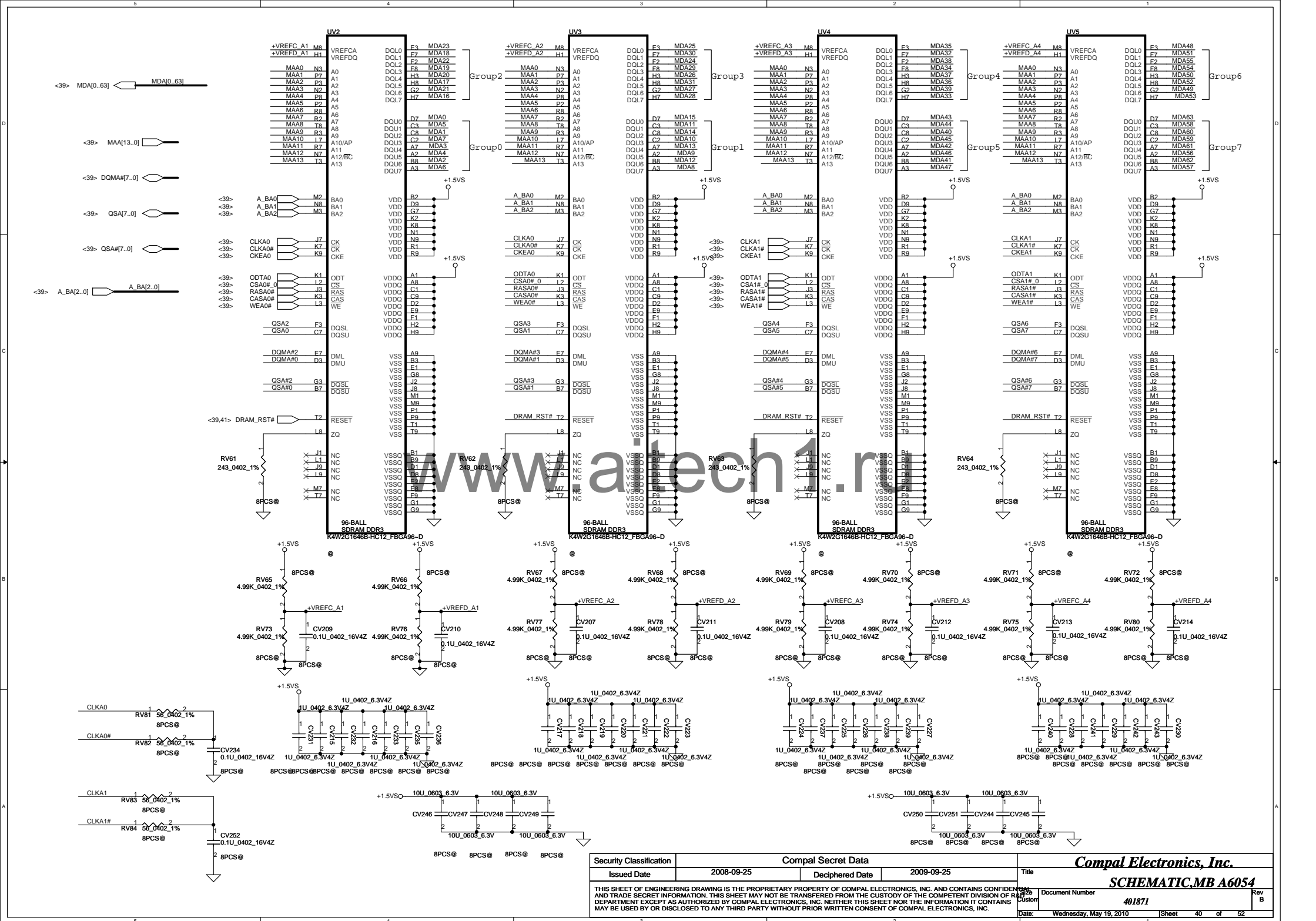
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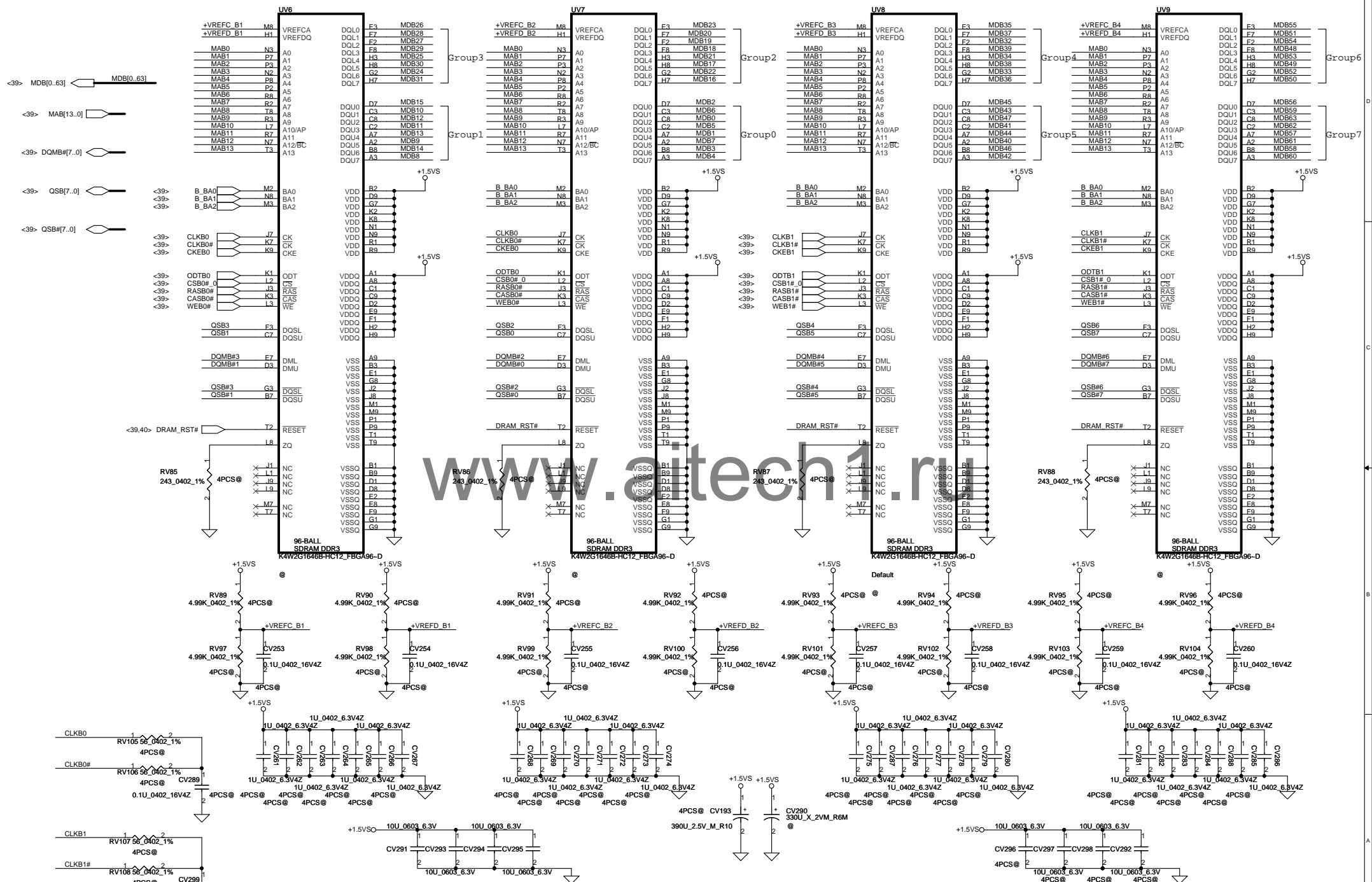


Park uses memory group B only



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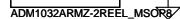
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GPIO_28_TDO GPIO21_BB_EN

UV1
Park
PARK@

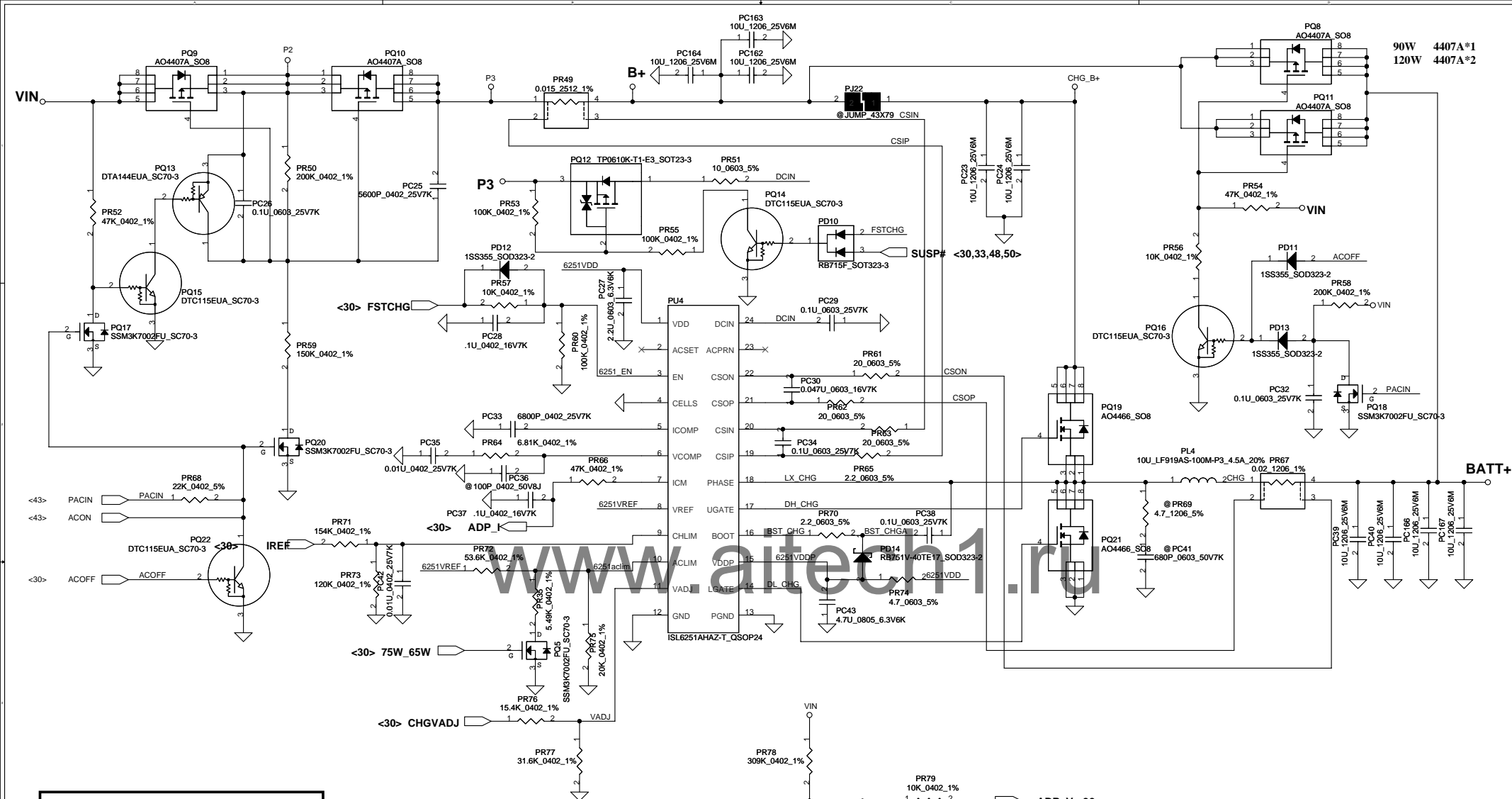
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```
Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)
```

[illegible]

Schematic diagram of the power supply section of the TP0610K-T1-E3_SOT23-3. The circuit includes a POK input, a voltage divider (PR47, PR48), a diode (PQ7), a resistor (PR45), a capacitor (PC19), and a diode (PQ6). The output is labeled B+O and +VSBP. Component values are specified: PR47 100K_0402_1%, PR48 0_0402_5%, PR45 22K_0402_1%, PC19 0.22U_0603_25V7K, PQ7 SSM3K7002FU_SC70-3, and PQ6 TP0610K-T1-E3_SOT23-3.

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CP mode
 $V_{aclim} = 2.39 * (R_b // 152K / (R_t // 152K + R_b // 152K))$
 $I_{input} = (1/PR49) * ((0.05 * V_{aclim}) / (2.39 + 0.05))$
 where $V_{aclim} = 0.6221V$, $I_{input} = 3.15A$
 $V_{aclim} = 1.09986V$, $I_{input} = 3.65A$
 $V_{aclim} = 0.7717V$, $I_{input} = 4.41A$
 $V_{aclim} = 0.4204V$, $I_{input} = 5.88A$

CC=0.25A-3.6A
 IREF=0.9133*Icharge
 IREF=0.228V-3.29V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.315V

CELLS	VDD	GND	Float
CELL number	4	3	2

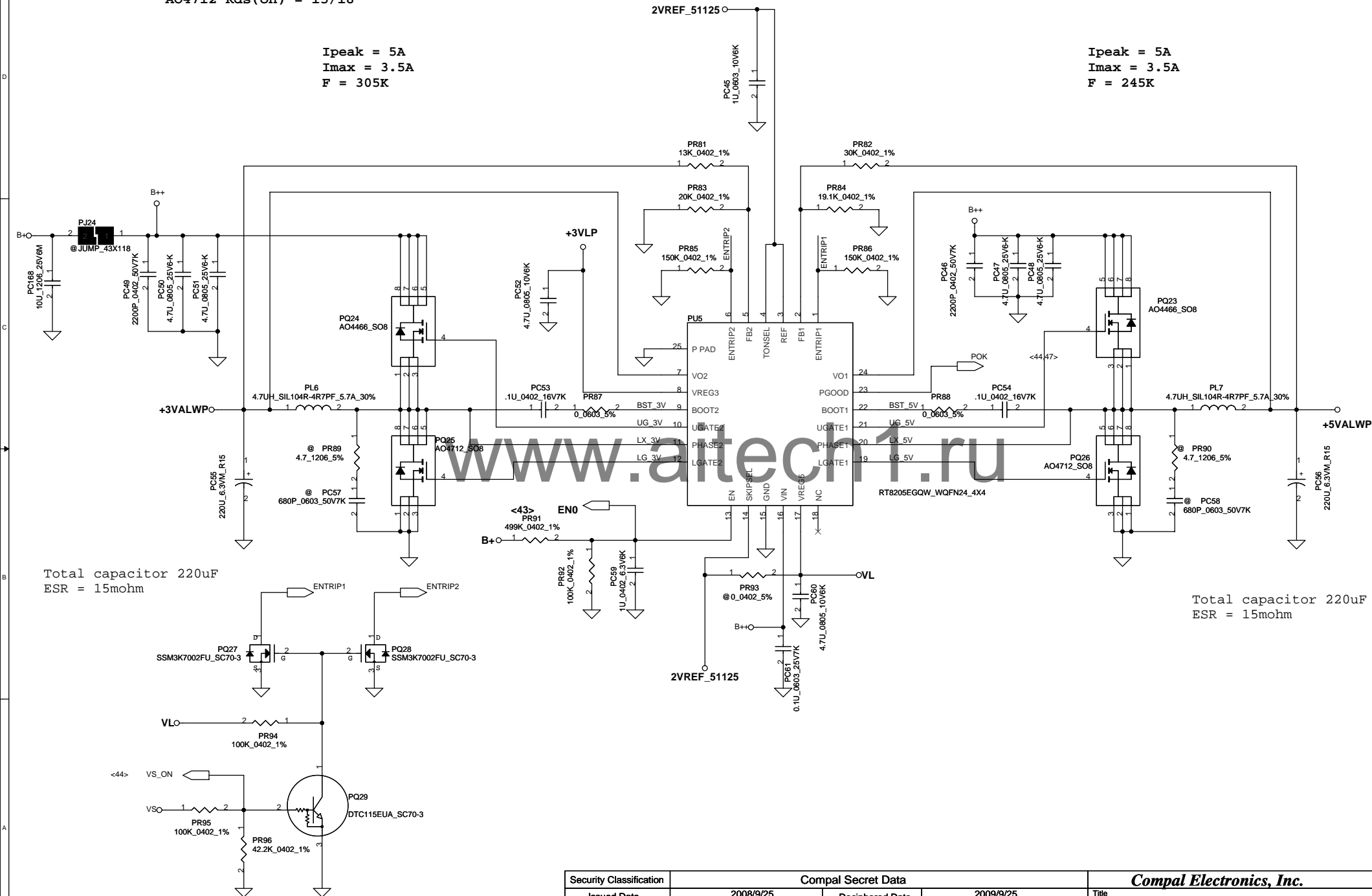
(75W) $I_{in} = 2.512 ADP_I$
 (120W) $I_{in} = 3.35 ADP_I$
 $V_{in} = 7.57 ADP_V$

$I_{ada} = 0-3.421A(65W)$ CP=3.15A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W_65W=high
 $I_{ada} = 0-3.947A(75W)$ CP=3.63A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W_65W=low
 $I_{ada} = 0-4.737A(90W)$ CP=4.36A PR49=0.015, PR72=53.6k, PR75=20k, PR35=unpop, PQ5=unpop
 $I_{ada} = 0-6.316A(120W)$ CP=5.81A PR49=0.015, PR72=8.25k, PR75=26.7k, PR35=unpop, PQ5=unpop
 CP= 92%*Iada

AO4712 Rds(on) = 15/18

Ipeak = 5A
Imax = 3.5A
F = 305K

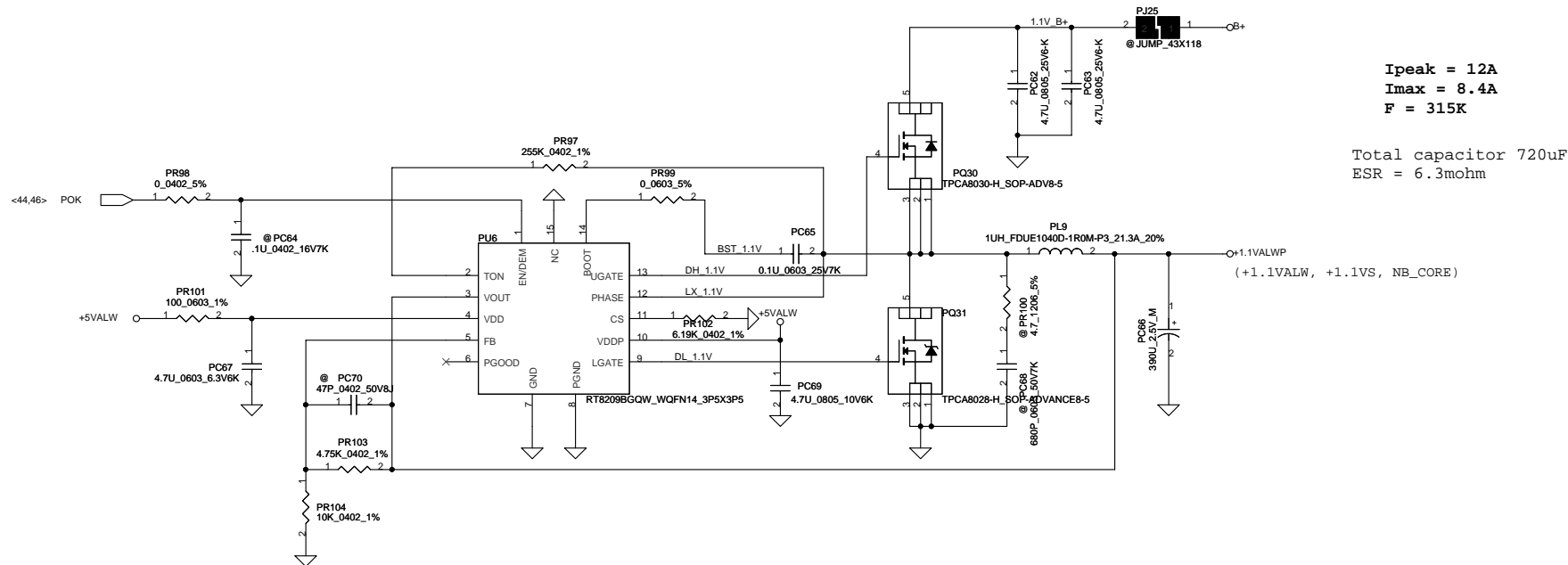
Ipeak = 5A
Imax = 3.5A
F = 245K



Total capacitor 220uF
ESR = 15mohm

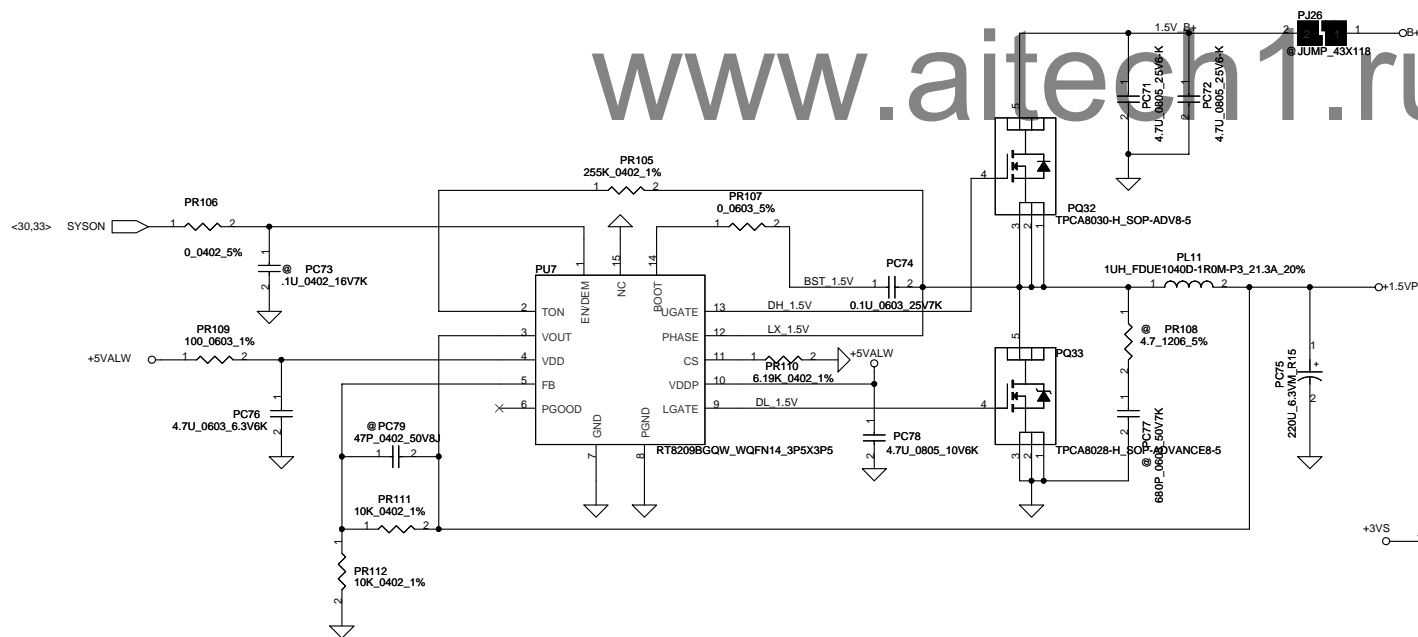
Total capacitor 220uF
ESR = 15mohm

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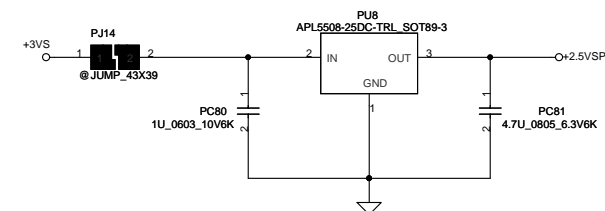
I_{peak} = 12A
I_{max} = 8.4A
F = 315K

Total capacitor 720uF
ESR = 6.3mohm



I_{peak} = 11A
I_{max} = 7.7A
F = 315K

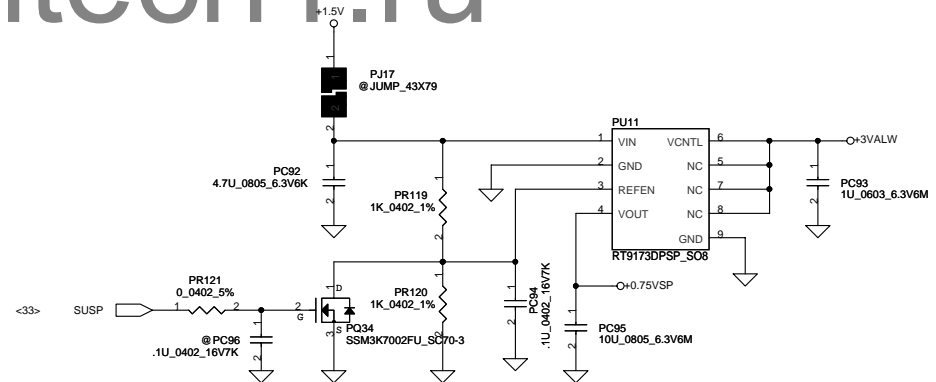
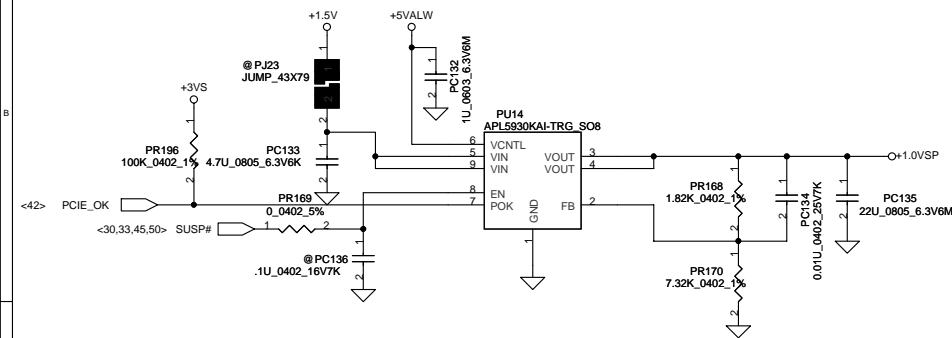
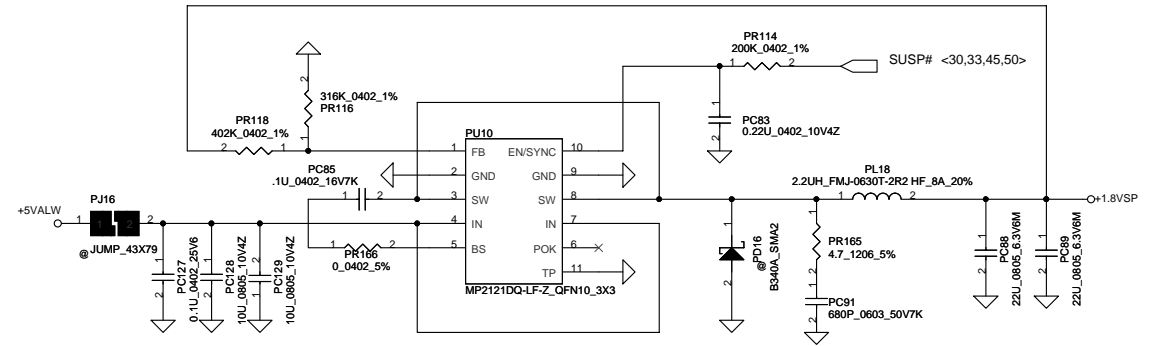
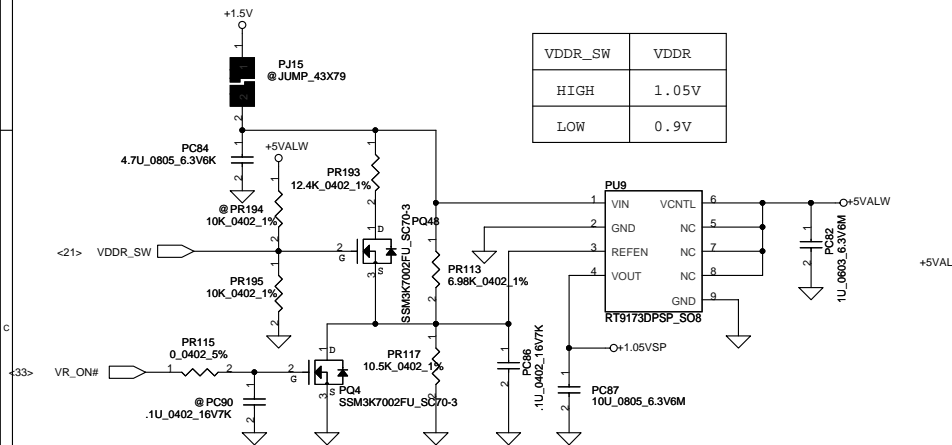
Total capacitor 1390uF
ESR = 2.73mohm



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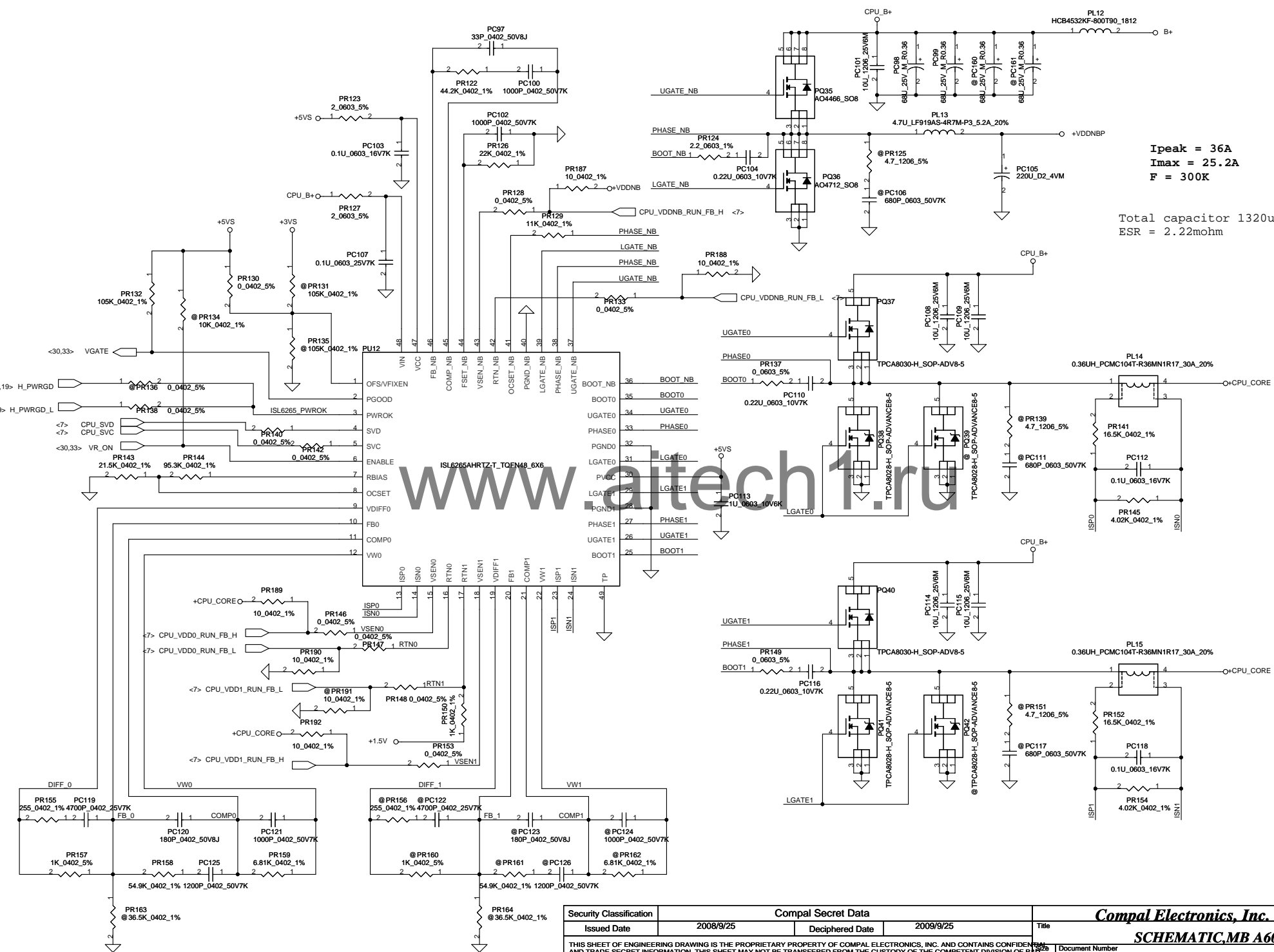
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VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V



Madison / Park PCIE : 1.0V	M96 / M92 PCIE : 1.1V
PR170 = 7.32K	PR170 = 4.75K

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Ipeak = 36A
Imax = 25.2A
F = 300K

Total capacitor 1320uF
ESR = 2.22mohm

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Rev B

PIR (Product Improve Record)
NALAE LA-6054P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	33	Change JLEDB pin define as customer request
2	2009/12/14	25,28,30	Delete JODDB, JBT and JUSBB support pin
3	2009/12/14	33	Change JPOWER Pin2 from GND to NC
4	2009/12/15	28	Add R95 at JWLAN Pin5 for BT/WLAN combo Mini Card
5	2009/12/15	25,30	Change U11, U25 P/N from SA00002XX00 to SA000033H00
6	2009/12/15	28	Reverse JBT pin definition
7	2009/12/16	27	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @
8	2009/12/17	33	Cyange JPOWER footprint to ACES_87151-1207_12P (ZIF_上接點)
9	2009/12/17	33	Cyange JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition
10	2009/12/17	33	Cyange JLEDB footprint to ACES_85201-1205N_12P (ZIF_上接點)
11	2009/12/17	25	Cyange JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)
12	2009/12/17	33	Change H36, H37 footprint from H_3P3 to H_3P8

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Version Change List (P. I. R. List) for Power Circuit

Page# Item Title Solution Description

DVT : modification from EVT

P47	change voltage divider to less than 10K	change PR104, PR111, PR112 to 10K; PR103 to 4.75K
P47	change 1.1V, 1.5V OCP value	change PR102, PR110 to 6.19K
P48	enlarge output cap	change PC88, PC89 to 22uF(S80000000I10)
P49	don't use NIPPON cap	change PC98, PC99 to SF0000000S80
P49	pull high RTN1 1.5V	change PR150 to mount
P50	APW7138 pin6 is NC	change PR179, PC154, PC156 to unmount
P46	choke need to meet thermal module height	change PL6, PL7 to SH000006380
P45	change system power from 90W to 120W	change PR72 to 8.25K, PR75 to 26.7K; PQ11 to mount
P49	production line request	change PC98, PC99 to 68uF; add PC160, PC161 68uF
P45	EMI request for ISN issue	add PC162, PC163, PC164 10uF 1206
P48	mount snubber circuit	mount PR165, PC91
P44	OTP setting common	change PR30 and PR31 to 19.6K; PR34 to 7.87K; PR33 to 8.66K
P48	change IC to low cost	change PU9 and PU11 to RT9173
P48	change VDDR(1.05V) circuit to switchable	add PR193, PR194, PR195 & PQ48

PVT : modification from DVT

P49	cost down	change PC98, PC99, PC160, PC161 to SF000000W00
P46	common circuit	change PC45 to 1uF
P46	common circuit	mount PC59
P46	change PQ29 solution	change PQ29 to DTC1158UA
P45	add 65W/75W selection circuit	Add PR35 and PQ5, unmount
P47	prevent OVP for HW's cost down	change PC66 to 390uF
P48	PCIE_OK pull high +3VS	add PR196=100K
P50	For 7138 output sensing stability	add PC165=1000p unmount
P45	EMI request for ISN issue	Add PC166, PC167, 10uF 1206
P46	EMI request for ISN issue	Add PC168, 10uF 1206

PreMP : modification from PVT

P44	Thermal request change OTP	change PR30, PR31 to 23.7K; PR33, PR34 to 11.3K
P45	modify 65W/75W resistor	change PR72 to 53.6K; PR75 to 20K; mount PR35 and PQ5
P48	modify 1.05V voltage setting	change PR113 to 6.98K
P50	modify VGA_CORE Choke	change PL17 to SH120568M00
P43	modify RTC circuit	

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